International Journal of Electrical and Electronics Engineers
Vol. No.8 Issue 01, January-June 2016
www.arresearchpublication.com
IJEEE
ISSN 2321 - 2055

10/100 MBPS ETHERNET MAC CORE DESIGN

M. Himaja

Assistant Professor, Department of EEE,

Prince Dr. K.Vasudevan College of Engineering and Technology, Ponmar, Chennai, TN

ABSTRACT

Ethernet is the commonly Used network standard when connecting to a Local Area Network or the Internet, When connecting an Embedded system to a LAN even just for point to Point communication, it was necessary to use additional network circuits that had more functionality than required, which came at a high cost .furthermore a processor was needed to implement the network stack. Three different udp/ip stack cores, with different grades of parallelism and suited for various network demands are implemented and analyzed. This is implemented on FPGA and focuses on the Tcp/Ip sub functions; the performance critical functions that can be accelerated in FPGAs.The Udp/ip area can be reduced to 1/3 of the original size with an appropriate implementation, accomplished by a tradeoff between parallelism, latency and area

Keywords*: *CSMA , FPGA, MAC, MII, UDP

I. INTRODUCTION

There are different types of communication

1. Point to point communication:

This refers to a connection restricted to two end points

2. Point to multipoint communication:

This provides multiple paths from a single location to multiple lacations.IT is used in wireless internet.

CSMA/cd Shared Medium Ethernet:

According to OSI (Open System Interconnection, Open Systems Interconnection) seven-layer network model, the key of Ethernet technology is the physical layer and the data link layer, where data link layer includes the media access control MAC (Medium Access Control) sub-layer and logical link control LLC (Logical Link Control) sub-layer, MAC sub-layer mainly contains the access content related to the transmission media, and which is independent in the actual network transmission. Therefore, it has important significance for the study of Ethernet MAC layer protocol.

Ethernet originally used a shared coaxial cable winding around a building or campus to every attached machine Carrier sense multiple access with collision detection Governed the way the computers shared the channel This is simpler than the competing token ring or token bus technologies. Even a computer want to send some information, it used the following algorithm:

MAIN PROCEDURE:

1. Frame ready for transmission
2. Is medium Idle? I F not, wait until it becomes ready and wait the interference gap period(9.6Us in 10Mbit/s Ethernet)
3. Start transmitting

International Journal of Electrical and Electronics Engineers
Vol. No.8 Issue 01, January-June 2016
www.arresearchpublication.com
IJEEE
ISSN 2321 - 2055

4. Did a collision occur/If so, go to collision detected procedure.
5. Reset transmission counters and end frame transmission.

COLLISION DETECTED PROCEDURE

1. Continue transmission and minimum packet time is reached (Jam signal) to ensure that all receivers detect the collision
2. Increment retransmission counter
3. Was the maximum number of transmission attempts reached, if so abort transmission
4. Calculate and wait random back off period based on number of collisions

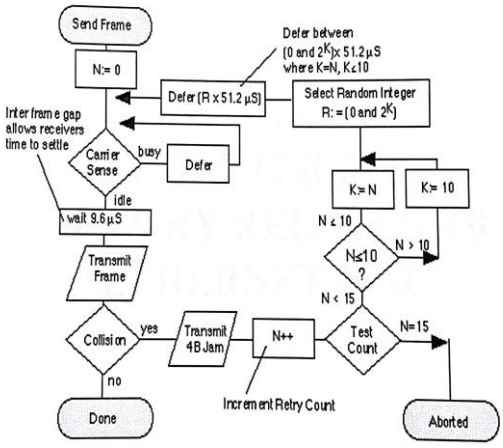

Figure 1:CSMA/CD Algorithm

Frame structure of Ethernet Mac core is :

7 bytes	1 byte	2 or 6 bytes	2 or 6 bytes	2 bytes	>=0	>=0	4bytes
preamble	sfd	Destination Address	Source Address	Length	LLC data	pad	FCS

Preamble:

A 7 bytes pattern of alternating 0's and 1's used by the receiver to establish bit synchronization**.**

Start of frame delimiter:

The sequence 10101011, which indicate the actual start of the frame.

Destination Address:

Specifies the station for which the frame is intended. It may be a unique physical address, a group address or a global address.

Source Address:

Specifies the station that sent the frame. Length: length of the LLC data field.

LLC data:

Data unit supplied by logic link control (LLC).

Pad:

Bytes added to ensure that frame is long enough for proper collision detection operation.

Frame Check Sequence (FCS):

International Journal of Electrical and Electronics Engineers
Vol. No.8 Issue 01, January-June 2016
www.arresearchpublication.com
IJEEE
ISSN 2321 - 2055

A 32 bit cyclic redundancy check, based on all fields except the preamble, sfd an FCS

II. ABOUT ETHERNET-MAC

Ethernet IP Core consists of 5 modules as shown in fig.1.

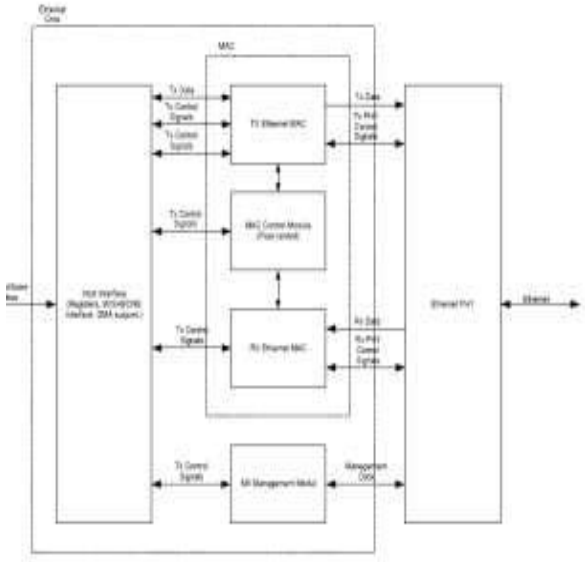

Figure 2: Architecture

ETHERNE MAC:

Ethernet is a family of frame based computing networking technologies for local area networks. A Frame is a digital transmission unit or data packet that includes frame synchronization that is a sequence of bits or symbols making it possible for the receiver to detect the beginning and end of the packet in the stream of symbols or bits. If a receiver is connected to the system in the middle of a frame transmission, it ignores the data until it detects a new frame synchronization sequence.

Architecture:

Ethernet ip core consists of 5 modules

1. Host interface and the BD structure
2. TX Ethernet Mac (Transmit Function)
3. RX Ethernet Mac (receive function)
4. Mac control module
5. MII Management module

HOST INTERFACE:

The host interface is connected to the risc and the memory through the wishbone. The risc writes the data for the configuration registers directly, while the data frames are written to the memory. Frames are accessed through the DMA

TX ETHERNET MAC:

Tx Ethernet mac generates 10 BASE_T/100 Base_Tx Transmit nibble data streams in response to the byte streams supplied from the transmit logic (host).it performs the deferral and back off algorithms, takes care. For the ifg, computes the checksum (FCS) and monitors the physical media.

RX ETHERNET MAC:

RX Ethernet Mac interprets 10 Base_t/100 Base_TX Mii receive data nibble stream and supplies correctly formed packet byte streams to the host

MAC CONTROL MODULE:

The function of this module is to implement the full duplex flow control .the Mac control module consists of three sub modules that provide the following functionality

1. Control frame detection
2. Control frame generation
3. TX/RX Ethernet mac interface
4. Pause Timer
5. Slot timer

CONTROL FRAME DETECTOR:

Checks the incoming frames for the control frames. Control frames can be discarded or passed to the host. When a pause control frame is detected, It can stop the transmitter module from transmitting for a certain period of time

CONTROL FRAME GENERATOR

When there is a need to stop the transmitting station from the transmission, a pause control frame can be used to send to it

TX/RX ETHERNET MAC INTERFACE

Mac control module is connected between the host interface and the transmitter and the reciever Mac modules. Signals from the host are passed by to the transmitter mac

PAUSE TIMER:

When a pause control frame is received, the pause timer value is written to the pause timer. This prevents the Tx module from transmitting for a pause timer value

Period of time

SLOT TIMER:

Slot timer measures the time slots and generates a pulse to the pause timer for every slot time passed by MII management module:

The function of this module is to control the phy and to gather the information from it

The MII management module consists of four sub modules:

1. Operation control module
2. Output control module
3. Shift register
4. Clock Generator

OPERATIONAL CONTROL MODULE:

The function of this module is to perform the following commands

1. Write control data
2. Read status
3. Scan status

Output control module:

1. Controls the signal appearance on the Mdo, Mck and mdoen pins

2. Shift register

Holds the status read from an external physical

3. Clock generator

Generates an appropriate output clock mck according to the input host clock and the clock divider bits

2.1 Transmitter Ethernet Mac

Transmitter Ethernet Mac implements csma/cd protocol When transmitting packets of data .Before transmitting packets of data, Transmitter Ethernet mac must ensure that medium is idle and then monitors medium continuously if there is a collision in the middle of transmit process. If collision happened, transmitter ethernet mac makes back off operation and retries to transmit after a random period depends on number of collision attempt

The transmit operation can be aborted if one of the following conditions is detected

1. Excess deferral, occurs when transmitter Ethernet mac can't get the opportunity to transmit longer than twice maximum length of Ethernet frame

2. Late collision, occurs when collision is detected after 512 bits of data has been transmitted excessive collision Occurs when collision is detected more than 15 times

3. Under run, occurs when host can't provide nibbles of data for transmit operation

4. Excessive length, occurs when the length of packet is longer than 1518 bytes

5. Clock is provided by mii through transmitter clock which frequency is 2.5MHz when operates at 10Mbps and 25 MHz when operates at 100 Mbps

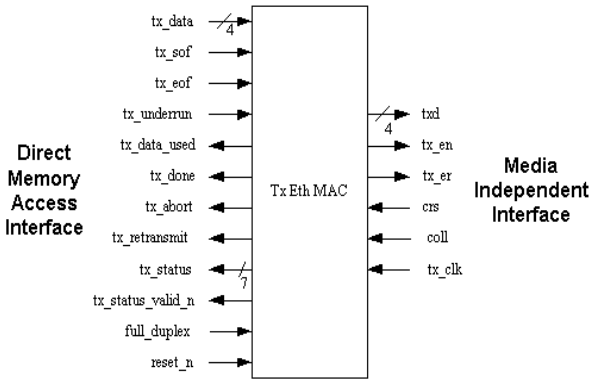

Figure 3:Transmitter Mac Module

Transmitter Ethernet mac consists of eleven modules

1. FIFO SYNCHRONIZATION:

The function of this module is to keep synchronization all outputs with the rising edge of input clock

2. INTER FRAME GAP TIMER

The Function of this module is to assure time interval between two packets of data or inter Frame gap is 96 bit time or 24 clock cycles

3. DEFER COUNTER:

The function of this module is to limit defer time for waiting opportunity to transmit a packet of data

4. FRAME LENGTH COUNTER:

The function of this module is to count the length of frame has been transmitted to mii.The length counter counts the length of frame while transmit_enable is detected and will be reset if transmit_enable is not asserted

5. COLLISION COUNTER:

The functions of this module are to count collision events, inspect number of consecutive collisions, and detect late collision

6. RANDOM NUMBER GENERATOR:

This module generates random number using linear feedback shift register which contains 10 bit register.This random number generator will select random number from range between 0 to (2^K)-1 with K is a smaller number between number of collisions and 10

7. BACK OFF TIMER;

The function of this module is to determine interval time for back off operation after a start_back off is detected. This interval time is calculated from multiplication between random number and slot time, that is random*128 clock cycles

8. JAM TIMER:

The function of this module is to determine how long JAM pattern has been transmitted

9. CYCLIC REDUNDANCY CHECKER:

The function of this module is to generate crc number, which will be added to Ethernet frame as fcs field

10. DATA MULTIPLEXER

The function of this module is to determine which data nibbles will be transmitted to mii, which are related to data_select signal from state machine

11. TRANSMITTER STATE MACHINE:

The function of this module is to control transmit process

Status signal	Description
Tx_status[0]	Excess deferral
Tx_status[1]	Late collision
Tx_status[2]	Excessive collision
Tx_status[3]	Transmit under run
Tx_status[4]	Excessive length
Tx_status[5]	Transmit abort
Tx_status[6]	Transmit success

Table 1: Summary of signals of state machines

2.2 Reciever Ethernet Mac

The Rx Ethernet mac block is responsible for recieving data and implements csma/cd protocol.The recieve process can be aborted or dropped if one of the following conditions is detected

1. Reset signal detected
2. Maximum frame length exceeded
3. Media error has occurred in the frame presently being receiver

International Journal of Electrical and Electronics Engineers
Vol. No.8 Issue 01, January-June 2016
www.arresearchpublication.com
IJEEE
ISSN 2321 - 2055

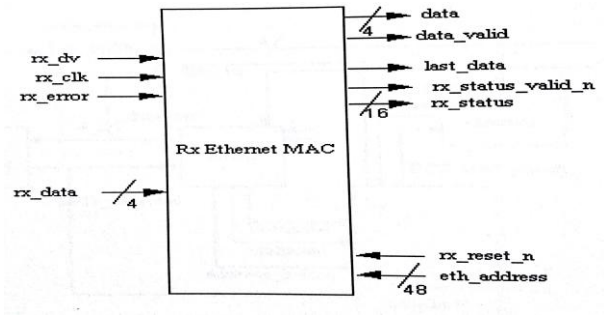

Figure 4: Reciever Mac Module

Receiver Ethernet Mac consists of 5 Modules

RX STATE MACHINE:

1. Controls receive process, the process starts when rx_dv asserted, that indicates packet data is coming to receive mac, then it activates start frame delimiter detector

2. After start frame delimiter is detected, the frame is hold in buffer, and delivered to FIFO

3. Meanwhile, destination address field and crc field are being checked

4. At the end of reception the Rx state machine marks the packet received by setting the appropriate bits in the receive status signals.

SFD DETECTOR:

1. Compares the destination address of the received packet to Ethernet address

2. The address matching logic is organised to hold six byte address entries

RX BUFFER:

1. Holds the frame being received, before they are transferred to FIFO

Signal	Type	Description
Rx_dara[3:0]	in	Data transferred from mii
Data[3:0]	out	Data transferred from buffer to FIFO
Data_tap[3:0]	out	Data transferred from buffer t o sfd detector and address matching logic
Data_en	in	Enable signal from rx state machine to open the buffer and lets data[3:0] delivered to FIFO
Rx_clk	in	Clock signals from Mii
Reset_n	in	Active low signals that initialises the receive mac function

Table 2: signal descriptions of Rx Buffer

International Journal of Electrical and Electronics Engineers
Vol. No.8 Issue 01, January-June 2016
www.arresearchpublication.com
IJEEE
ISSN 2321 - 2055

FCS CHECKER:

Computes a crc across the decapsulated frame to find the magic number. Ethernet uses a Cyclic Redundancy Check (CRC) algorithm to detect transmission errors. The Frame Check Sequence field is filled (using a CRC) by the sending host. If the receiving host detects a wrong CRC, it will throw away that packet.

III. RESULTS AND CONCLUSIONS

We have proposed and implemented transmitter and receiver Ethernet Mac modules by using verilog. we have verified the individual modules of the transmission by using error detection code crc and type of collision occurred during the transmission. At the receiver the received frame address compared with Ethernet address by using address match logic to identify whether the Received frame is unicast, multicast or broadcast. The Simulation results for transmitter state machine and receiver state machine are an analysed

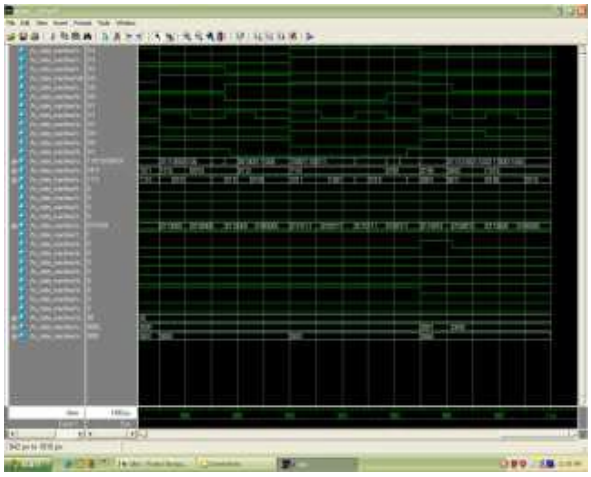

Figure 4: Transmitter Ethernet mac simulation results

Figure 5: Transmitter Ethernet mac simulation results

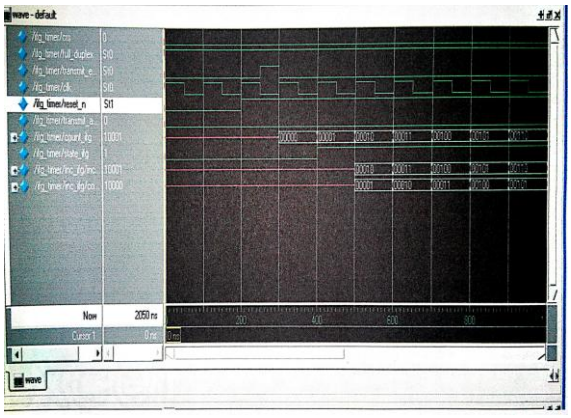

Figure 6: Ifg timer

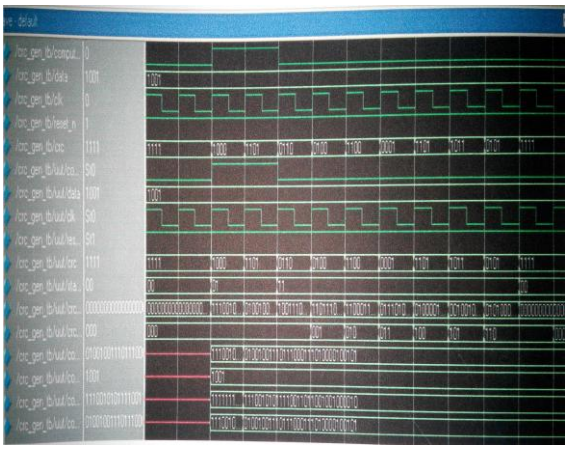

Figure 7: crc generator

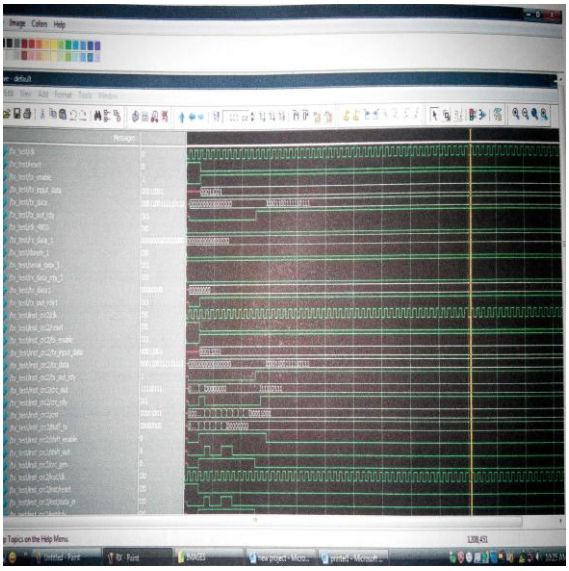

Figure 8: Receiver state machine

ACKNOWLEDGMENTS:

I would like to thank my guide Karunakar, Asst professor, GitamUniversity, Andhrapradesh for supporting me throughout the project

REFERENCES

[1] J. Xu and Q. S. Lin, "*Design and Implementation of Ethernet MII Interface Extension Based on FPGA",* Electronic Design Applications, vol. 7, (2011).

[2] X. R. Xie, "*Computer Network",* Electronic Industry Press, Beijing (2003), pp.92-120.

[3] Z. S. Zhang and Y. L. Huang, "Research *and Application of Embedded Ethernet data Acquisition System"*, Computer Systems and Applications, vol. 7, no. 19, (2010).

[4] J. Q. Li and X. G. Zhang, "*Design of Smart Home Monitoring System Based on Cortex-M3*", Modern Electronics Technique, vol. 7, no. 35, (2012).

[5] J. Bhasker, "*Verilog HDL Hardware Description Language",* Mechanical Industry Press, Beijing (2000).

[7[] J. Liu, *"Design of Embedded NC System Based on ARM and FPGA",* Harbin Institute of Technology, (2013), June.

[8] D. Li and C. Chen, "*Research and Implementation of High-Speed Serial Transmission Interface Based on FPGA"*, Aeronautical Computing Technology, vol. 2, no. 38, (2008).