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DESIGN AND ANALYSIS OF LOW- POWER, AREA-EFFICIENT COMPARATORS

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ABSTRACT

The use of high speed, less delay, area efficient and low power analog to digital converter is impelling towards the clocked regenerative comparators. In this paper transient analysis of clocked regenerative comparators are done and on the basis of analysis result, a new dynamic comparator is designed.

Proposed comparator consumes less power as compared to conventional comparators and concluded in nano seconds which shows the speed. Technology used is 0.18-um CMOS technology.

Keywords: ***Clocked Regenerative Comparators, DTC, Layout, Low-Power.***

I. INTRODUCTION

On the basis of operation, nature, and inputs, comparators are of many types like voltage and current comparators, continuous and discrete time comparators etc. Some of the applications of comparators are analog-to-digital conversion, signal detection and function generation. Comparator is an important part of analog to digital converters. Nmos high speed comparator, pmos high speed comparator and wide swing comparator in analog Ultra Deep submicrometer Technlogies faces a problem i.e. Low power supply which means the threshold voltage of the devices is not scaled at the same rate as power supply is scaled. So it very challenging to design a comparator working on low power supply. To overcome this problem of supply voltage, double tail comparator are mostly used. [2] Many techniques, like supply boosting methods [3], [4], techniques employing body-driven transistors [5], [6], current-mode design [7]. dual-oxide processes technique can handle higher supply voltages which have been developed for the low voltage challenges in CMOS devices.

Comparator is a circuit that compares the analog signal with the another anolog signal and convert into the digital signal keeping its content unchanged. The basic operation is shown in Figure 1 (a),

Case-A.if Vp is greater than Vn, the output will be Logic zero.

Case-B. if Vp is less tha Vn, the output will be Logic one.

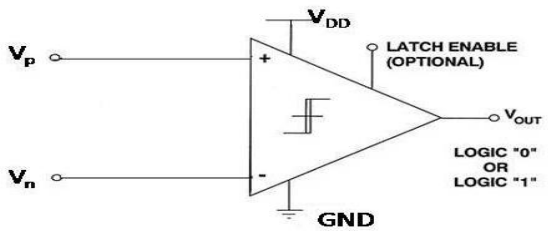

Figure 1 (a): Schematic of Comparator

Where Vp and Vn are the pulse voltage and reference voltage applied to the +ve and –ve terminal respectively. Figure 1 (b) shows the ideal characteristics of compa

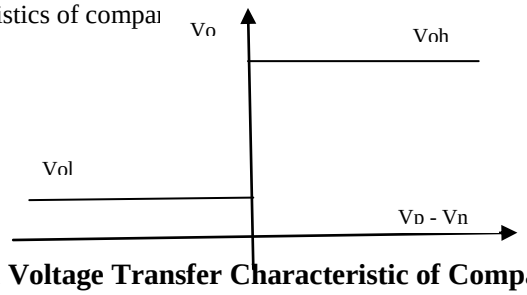

Figure 1 (b): Ideal Voltage Transfer Characteristic of Comparator

Comparator mainly consist of 3 stages : input stage, decision stage and output stages. Input stage also called as pre-amplifyng stage provides the sensitivity to signal by amplifying it. Decision stage, as its name implies it takes the decision about signals which one is greater and depending on the condition provide the result to the output stage. Output stage is used to represent the digital signal.[1] as shown in Figure 1 (c).

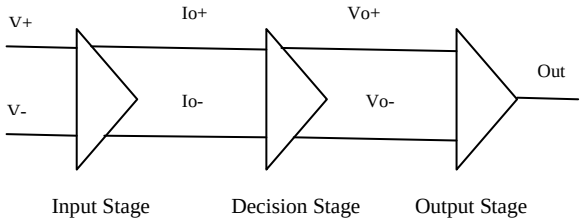

Figure 1 (c). Stages of Comparator

II. CLOCKED REGENERATIVE COMPARATORS

Clocked regenerative comparators are known for its speed because of strong positive feedback mechanism in the latch regeneration process. It is the only fact , these comparators are used in high speed analog to digital converters.[1] This process is explained in the conventional dynamic comparators and double-tail dynamic comparator below:

2.1 Conventional Dynamic Comparator

Conventional Dynamic Comparator is mostly used in the Analog to Digital Converters (ADC). Figure 1(a) shows the conventional comparator and its Operation is as below:

Case (a). When clk is in reset phase or equals to zero, transistor Mtail is OFF and pmos transistor (P1 & P4) turns ON which pulls the output Outp and Outn to Vdd.

Case (b). When clk is in condition phase or equals to 1, P1 and

P4 transistor turns OFF, Mtail is ON, Now Outp and Outn(output voltages) discharge depending on the input (Inn and Inp).

If Inn > Inp , Outn will discharge faster than Outp, when Outn discharged by nmos transistor N1 drain current, falls down to VDD–|Vthp| before Outn discharged by nmos transistor N4 drain current, it turns ON the pmos transistor P3, which starts the latch regeneration process (N3, P3 & N2 , P2). If Inp > Inn, working is vice versa. Figure 2 (b) and Figure 2(c) shows Layout and waveform of the Conventional Dynamic Comparator respectively.

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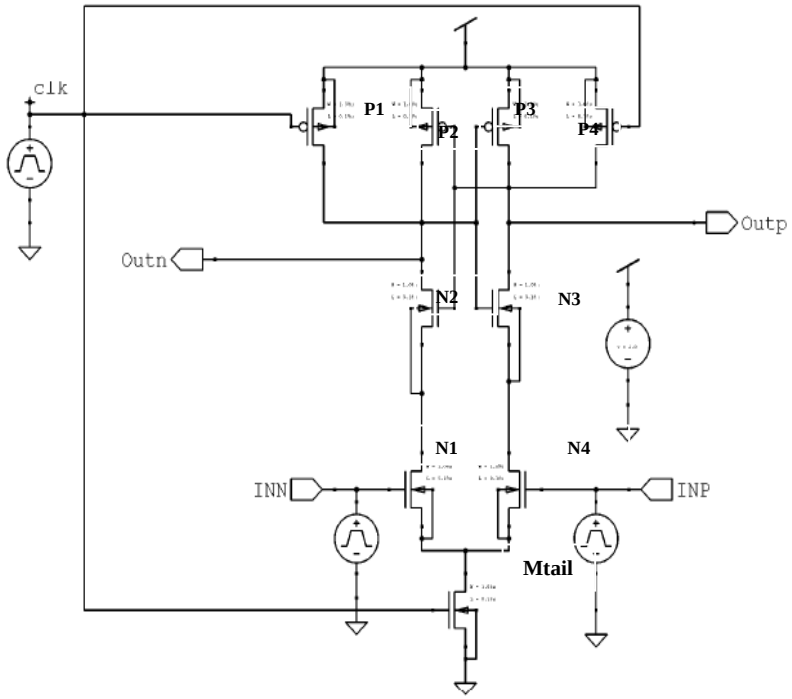

Figure 2 (a). Schematic of the Conventional Dynamic Comparator

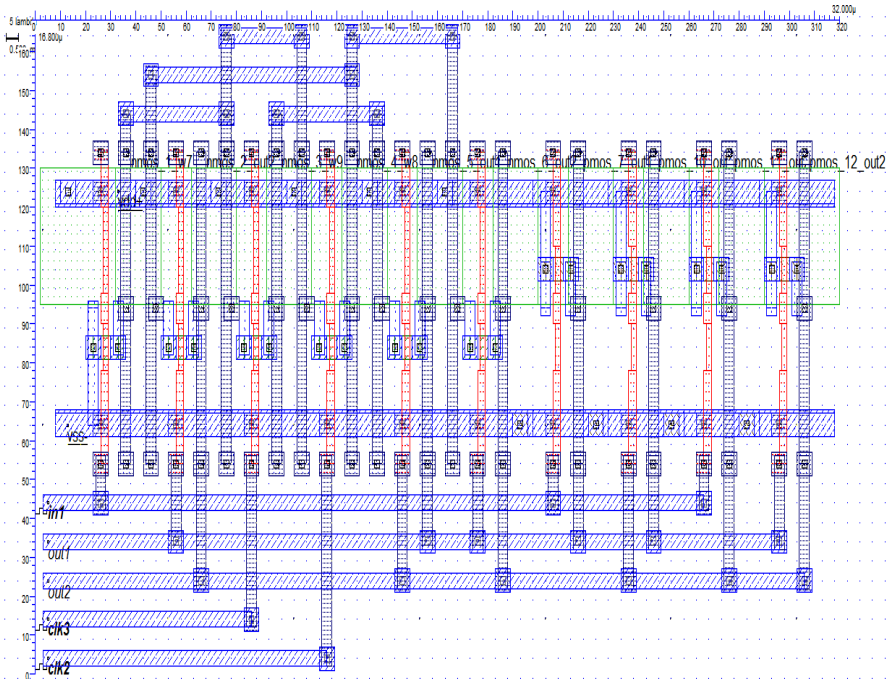

Figure 2 (b). Layout of Conventional Dynamic Comparator

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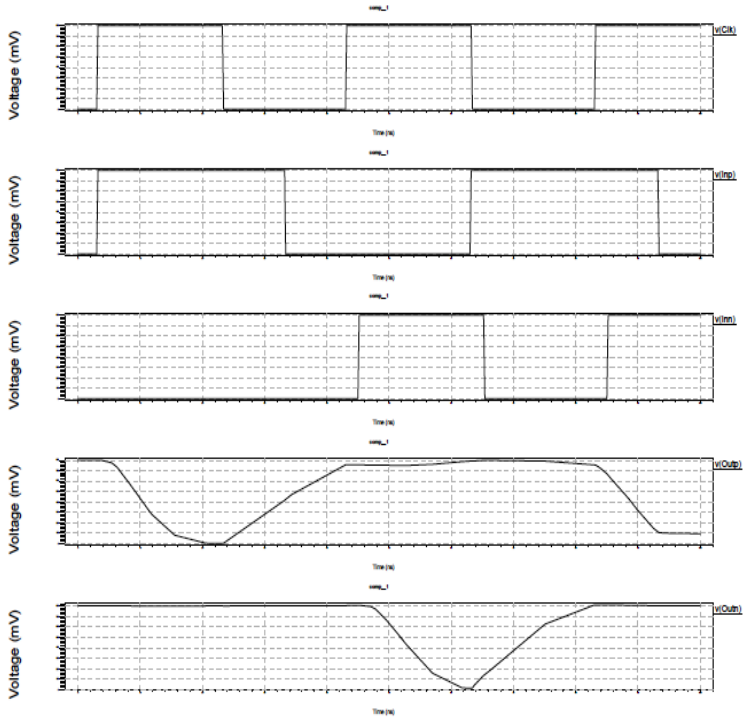

Figure 2(c). Waveform of Conventional Dynamic Comparator

2.2 Conventional Double-Tail Comparator

Due to less stacking, Double tail comparator can operate on low supply voltage.[11] Figure 3 (a) shows the conventional comparator and its Operation is as below

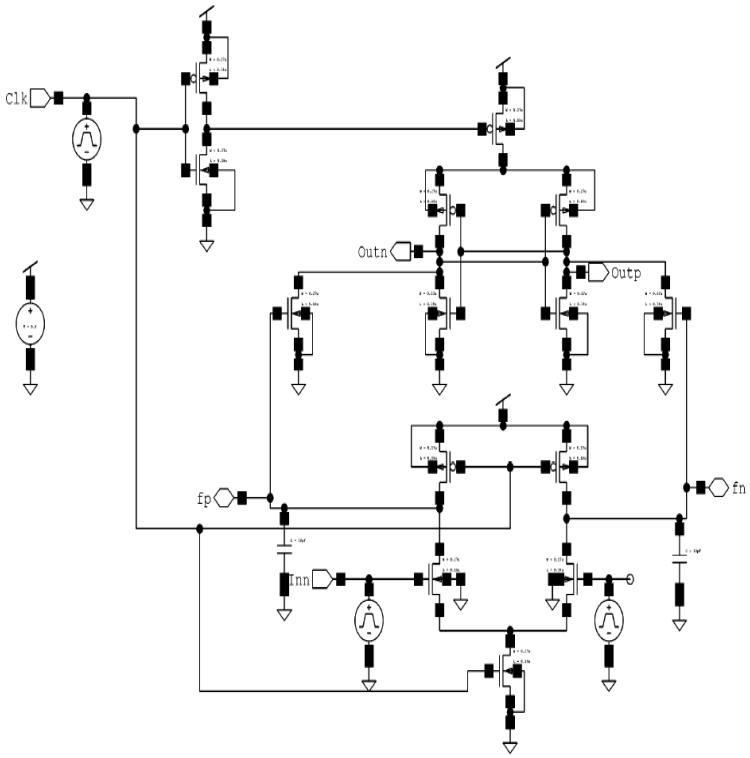

Figure 2 (d). Schematic of the Conventional Double-tail Comparator

Case (a). When clk is in reset phase or equals to zero, transistor Mtail1 and Mtail2 are OFF, pmos transistor P5 and P6 turns ON which pull the fn and fp to the Vdd. fn and fp are input to mR1 and MR2 respectively. So MR1 and MR2 gets ON and Outp & Outn pulls to Vdd. It is also called as precharge state.

Case (b). When clk is in condition phase or equals to 1, P5 and

P6 transistor turns OFF, Mtail1 and Mtail2 are ON, Now Outp and Outn(output voltages) discharge through fn and fp depending on the input (Inn and Inp). [2]

If Inn > Inp , Outn will discharge faster than Outp, it turns ON the pmos transistor P4, which starts the latch regeneration process (N5, P4 & N4 , P3). If Inp > Inn, working is vice versa. Figure 2 (e) and Figure 2(f) shows Layout and waveform of the Conventional Dynamic Comparator respectively.

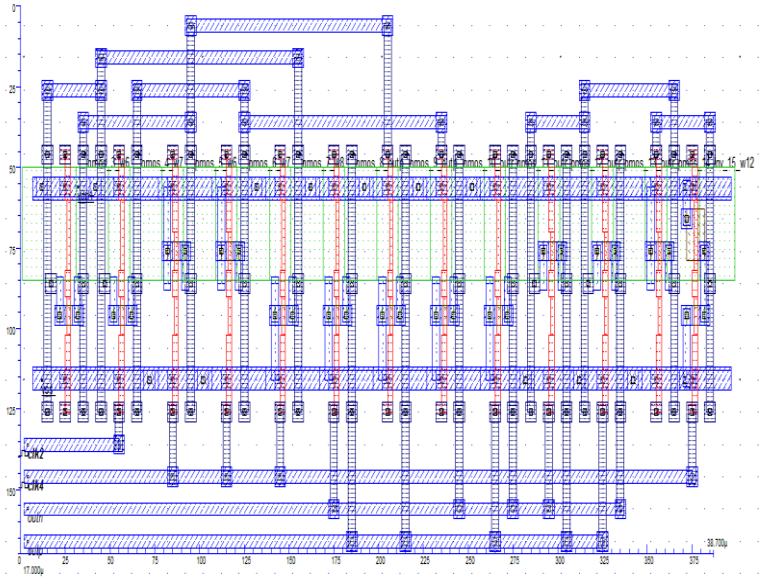

Figure 2 (e). Layout of Conventional Double-tail Comparator

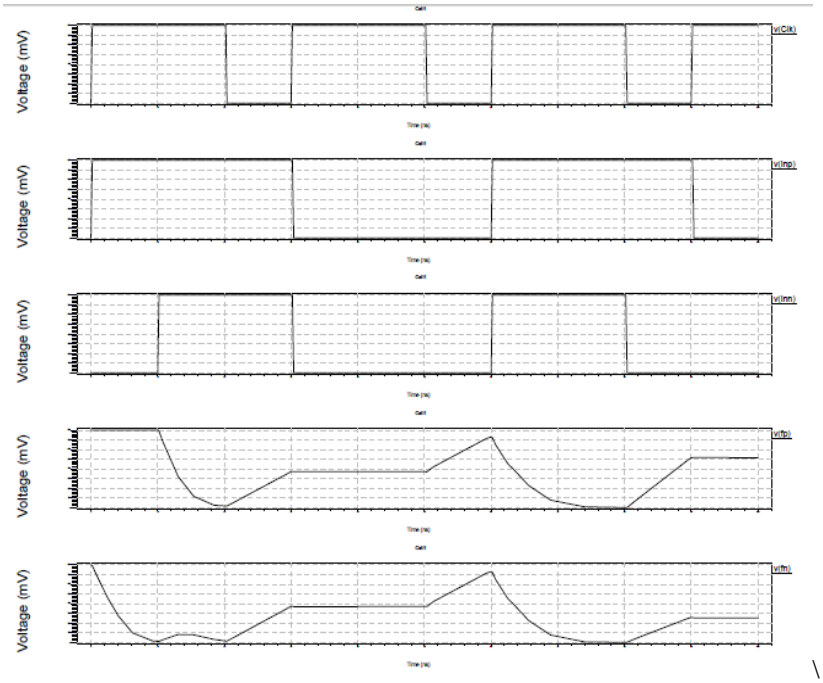

Figure 2(f). Waveform of Conventional Double-tail Comparator

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III. PROPOSED COMPARATOR

The schematic of Proposed dynamic comparator (PDC) is shown in figure 2(g). Operation of PDC is discussed below:

Case (a). When clk is in reset phase or equals to zero, transistor Mtail1 and Mtail2 are OFF, pmos transistor P4 and P7 turns ON and pull fn and fp to Vdd, P5 and P6 are in cut of region. P4 and P7 reset both latch to ground.

Case (b). When clk is in condition phase or equals to 1, P5 and P6 transistor turns OFF, Mtail1 and Mtail2 are ON, pmos transistor P4 and P7 turns OFF. At the beginning of this phase, fn and fp are about to Vdd depending on Inn and Inp. When Inp > Inn, fn drops at a rate faster than fp. As fn is falling, P5 will turn ON which pull fp to vdd. n turn off the transistor P6. It allow fn to be discharged completely. Latch regeneration time is decreased because of the difference between fn and fp. when one of the control transistors P5 or P6 turns on, a current from *V*DD is drawn to the ground via input and tail transistor (e.g., N5, Nsw1, and *M*tail1), this results in static power consumption. To overcome this issue, two nMOS switches are used below the input transistors [*N*sw1 and *N*sw2,]

As in reset phase, fn and fp pulls to Vdd. and condition phase when fn falling faster than fp. When fp pulls to Vdd, transistor Nsw1 turns off. And Nsw1 is in open state and fn drops completely.

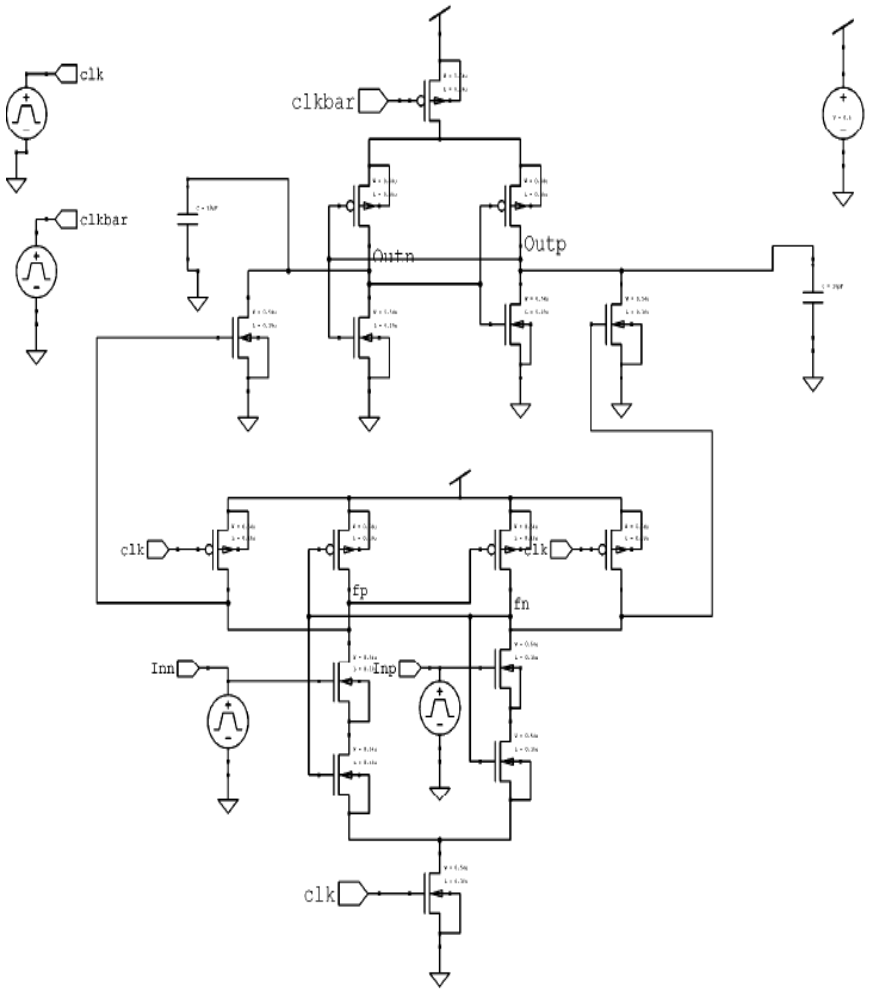

Figure 3 (a). Schematic of the Proposed Comparator

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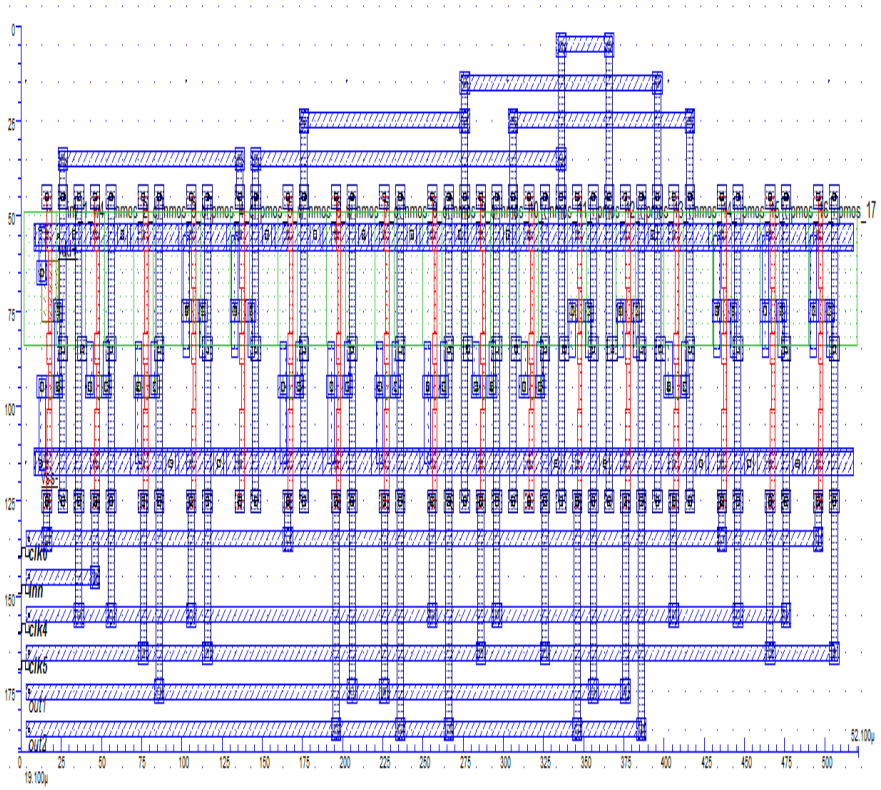

Figure 3 (b). Layout of Conventional Proposed Comparator

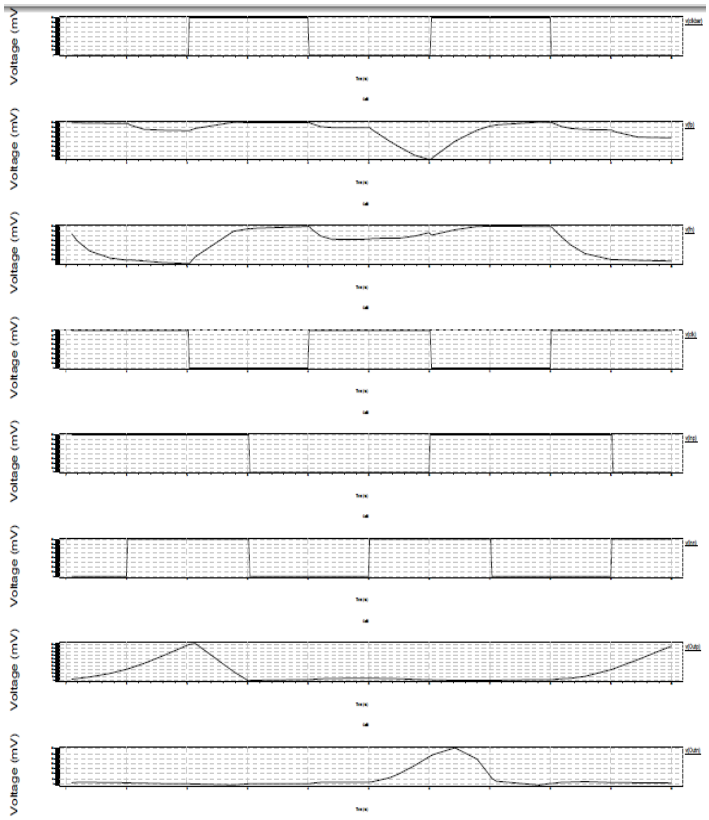

Figure 3(c). Waveform of Conventional Proposed Comparator

IV.RESULT

Comparison of these comparator is shown in the table below with respect to the parameters power consumption, delay and area.

Comparator Type	*POWER CONSUMTION (uW)*	*DELAY (n sec.)*	*AREA (um)²*
Conv. DC	4.80	7.29	726
DTDC	7.97	2.90	1040
Proposed Comparator	5.83	0.10	988

Table 1. Comparative Result of Various Comparators

V. CONCLUSION

In this paper, a comparator is designed which is best suited for analog to digital converters because of less power consumption, less delay and efficient area. Technology used is 180 CMOS technology in SPICE environment at 0.8V.

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