COMPARATIVE STUDY OF DOUBLE GATE SOI MOSFET AND SINGLE GATE SOI MOSFET THROUGH SIMULATION

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ABSTRACT

In this paper, 25 nm Single Gate Silicon on Insulator (SG-SOI) MOSFET is compared with Double Gate Silicon on Insulator (DG-SOI) MOSFET. The DG-SOI structure is similar to the proposed SOI with the exception of back gate at body. The resulted modified DG-SOI-MOSFET reduces the short channel effects (SCEs). The transfer characteristics DIBL, threshold voltage, I_{on} and I_{off} for 25nm are evaluated. The back gate structure of DG SOI is the mirror image of front gate SOI. The simulation is done using ATLAS simulator in SILVACO TCAD.

Keywords: Double Gate Silicon On Insulator (DG SOI), Single Gate Silicon On Insulator (SG SOI), Drain Induced Barrier Lowering (DIBL).

I. INTRODUCTION

Silicon CMOS technology has emerged over the last 25 years as the predominant technology of microelectronics industry due to large transistor density. CMOS technology was evolved by Moore's Law. Moore's Law is the succinct description of the persistent periodic increase in the level of miniaturization. The CMOS transistors gate length scaling is projected to continue from 2016 to 9nm [1].

MOS IC's have met the world's growing needs for electronic devices for computing, communication, entertainment, and other applications. When the MOS transistor dimension is scaled down to nanometer (<100nm), many physical barriers arise, like short channel effects, drain induced barrier lowering (DIBL), punch through, drain current, high leakage etc. due to large scaling, MOS transistor face the difficulties due to large leakage current which directly affect the process and degrades the device. For short channel, the magnitude of electric field increases in MOS, because terminal voltages are not scaled. To eliminate the submerged leakage path, an ultra-thin body structure is used.

In such a scenario, the Silicon-on-Insulator (SOI) technology come forward to become the next driver to continue the Moore's Law. The first partially depleted fabricated device was Silicon on Sapphire (SOS) at a sapphire substrate. But it is now, changed the insulator by Silicon Dioxide. SOI is designed in two types, Fully Depleted and Partially Depleted SOI. and the process variation, is observed due to which the use of Partially Depleted SOI come to an end. In order, to analytically model the 2D characteristics of short channel thin film SOI nanoscale MOSFET, the 2D poisson's equation must be solved.

Fully Depleted (FD) SOI device is widely used by chipmakers, at smaller gate length. FDSOI design on Silvaco is shown in Fig 1. On changing, Silicon or oxide length the performance of devices varies linearly. FDSOI exhibits superior transcondutance, current drive and subthreshold swing. But the leakage current and DIBL still continues. SOI provides the speed advantage, because the source/drain to body junction capacitance is eliminated. But the cost factor increases, that's why only high price microprocessor uses SOI. In future, SOI will get the more compelling application because of its flexibility.

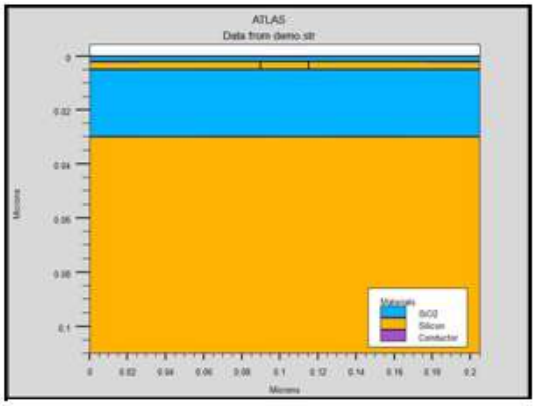

Fig 1 Structure of FDSOI on Silvaco

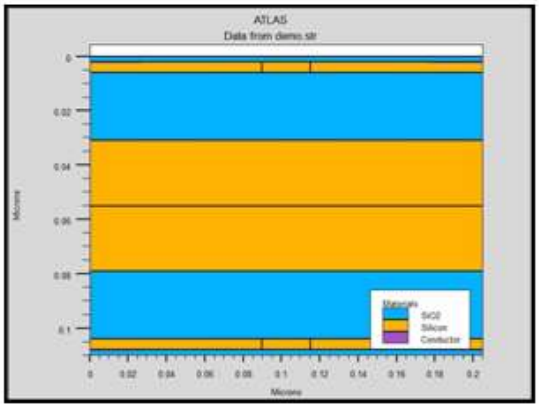

Fig 2 Structure of DG-FDSOI at Silvaco

To reduce the deep submerged leakage path, FDSOI is modified into Double Gate FDSOI. The back gate is added in FDSOI structure of similar dimensions of front gate which influences the operations of device .The two buried oxide (BOX) layer is separated by enough distance as to be independent of each other. This establish new device for low power applications with high performance. DG-FDSOI design on Silvaco is shown in Fig 2. separate electrodes are used for back structure of DG-FDSOI. The doping level of back structure is same as front one.

DG-FDSOI seem to a very promising option for ultimate scaling of CMOS [2]. Since, such type of structure provides a desirable threshold voltage (not too high or too low). It provides good short channel effect (SCE) immunity. SCEs also include the DIBL which is a threshold voltage (V_{th}) dependent and complicates the CMOS design. DG-FDSOI devise shows improvement over FDSOI single gate devices in area of high temperature. From the two gates, if only one gate is biased and other one is grounded then device will be in off state and will turn on only at biased position of both gates.

The important effects which are compared in this paper are DIBL, I_{on}, I_{off} and leakage. DIBL a SCE is calculated by

$$DIBL = \frac{\Delta V_{th}}{\Delta V_{ds}} = -[\frac{(V_{th1} - V_{th2})}{V_{ds1} - V_{ds2}}]$$

Where V_{th1} is the threshold voltage at drain voltage = 1V and V_{th2} is the threshold voltage at drain voltage = 0.5 V. at short channel, the drain depletion region comes closer to the source depletion region and field penetrates. When the injection of electrons by source increases, V_{th} shifts.

II. PHYSICAL PARAMETERS

The physical parameters of electrical characterization of SG SOI-MOSFET and DG SOI MOSFET are given in Table 1 and Table 2. Gate length for both device is 25nm. On comparing, the back gate DG FDSOI has same dimensions as front gate.

The designs are made in the ATLAS framework of SILVACO TCAD tool [3]. Device simulation is an important tool as it provides us quick feedback.

In this paper, we studied the characteristics of DG-FDSOI-MOSFET and SG SOI MOSFET for 25nm technology. The log values of I_D-V_G curve of DG-FDSOI-MOSFET and SG FDSOI MOSFET is shown in Fig 3 and Fig 4. Log curves are used to calculate the I_{off} value. The channel doping is uniform. Electric field structure of DG-FDSOI and SG FDSOI is shown in Fig 5 and Fig 6. Due to reduced vertical electric field, the gate current is suppressed [4].

Table 1

Physical Parameters	**Value**
Technology Node	25nm
Gate Oxide thickness	2 nm
T_{si} thickness	4nm
Source/Drain Doping	$9.56e16cm^{-3}$
BOX thickness	25nm
Substrate thickness	95nm
Channel Doping	$3.5e11cm^{-3}$
Substrate Doping	$1e10cm^{-3}$

Threshold voltage for both devices is calculated by the graphical approach. Thinner the oxide layer, lesser the

Table 2

change in threshold voltage. On increasing initiated drain voltage, the threshold voltage reduced.

Physical Parameters	**Value**
Technology Node	25nm
Back Gate Oxide thickness	2nm
Front Gate Oxide thickness	2 nm
T_{si} thickness (front)	4nm
T_{si} thickness (back)	4nm
Source/Drain Doping	$9.56e16cm^{-3}$
BOX thickness (front)	25nm
BOX thickness (back)	25nm
Substrate thickness	48nm
Channel Doping	$3.5e11cm^{-3}$
Substrate Doping	$1e10cm^{-3}$

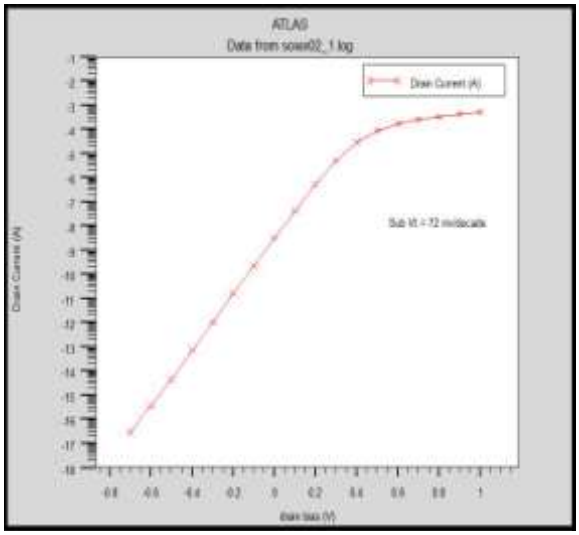

Fig 3. Log value of $I_D - V_G$ curve of DG- FDSOI-MOSFET.

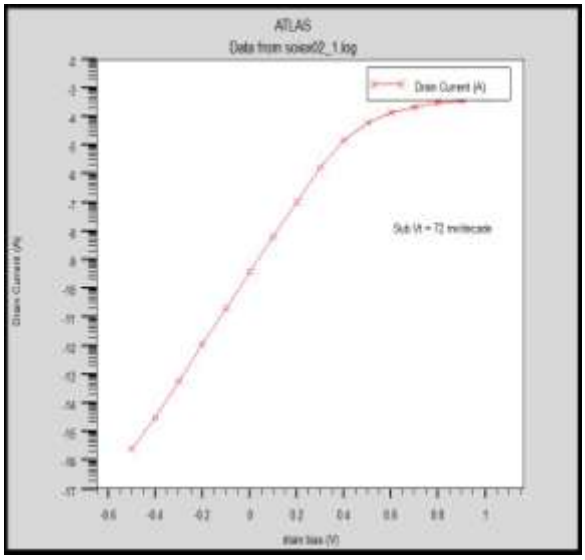

Fig 4. Log value of $I_D - V_G$ curve of SG FDSOI MOSFET.

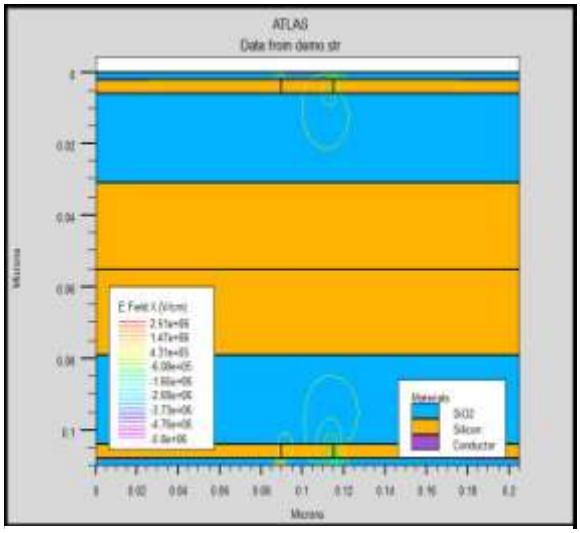

Fig 5. Electric field of DG FDSOI.

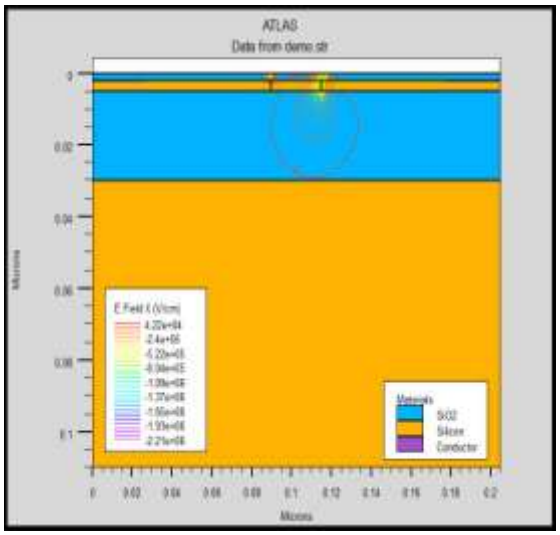

Fig 6. Electric field of SG FDSOI.

III. RESULT

The 2D device simulator is used to verify the proposed models. We have simulated the result of DG FDSOI device and FDSOI device. DG device demonstrate the close result to SG, but better than SG.

Table 3

Parameters	*SG-FDSOI*	*DG-FDSOI*
I_{on} *(at* V_d*=1V)*	506 µA	422 µA
I_{on} *(at* V_d*=0.5V)*	65.4 µA	48.3 µA
I_{off} *(at* V_d*=1V)*	0.470 nA	3.104 nA
I_{off} *(at* V_d*=0.5V)*	0.144 nA	0.895 nA
I_{on}/I_{off}	1265 X 10^3	136 X 10^3
DIBL	0.03	0.064

Table 3 shows the simulated results of both the devices. Table shows that on current of single gate SOI is larger than the DG FDSOI due to the large mobility of electrons in SOI in comparison of DG SOI. The drive current of both the device is compared in Fig 7 and Fig 8 at drain voltage 1V and 0.5V.

It can be seen that off state leakage current (I_{off}) is low in SG SOI because highly conducting surface acts as a barrier for electric field [5]. And electric field reduced at front gate of DG SOI but increased at back gate due to which the leakage current in DG FDSOI is high.

The two gates with two BOX causes the band gap reduction that reduces the silicon work function and increases the carrier concentration results in large DIBL.

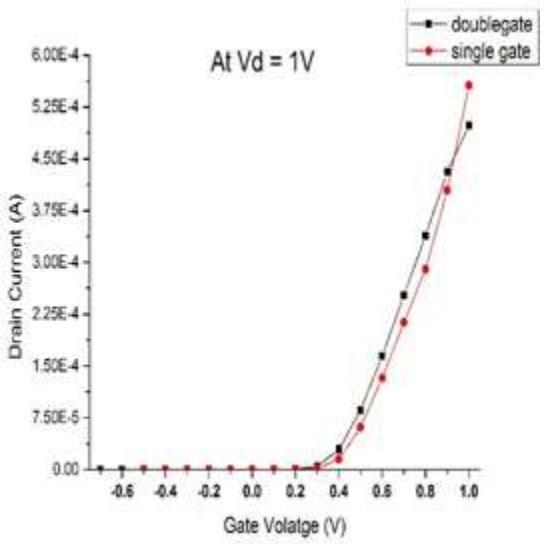

Fig 7. Comparison of I_D - V_G of DG FDSOI and SG FDSOI at V_D = 1 V.

IV. CONCLUSION AND FUTURE SCOPE

The nanoscale devices have SCEs like DIBL, hot carrier effect, due to which the device cannot be further scaled. So, this work is further demonstrated by designing two gates on same dimension of single gate. So that, the DG FDSOI performance enhanced and will work more efficiently.

We have investigated in detail the electrical characteristics of DG-FDSOI and FDSOI. Their drive current and DIBL is compared. The FDSOI has 506 µA whereas DG FDSOI has 422 µA i.e. FDSOI has larger drive current. Similarly, DIBL of FDSOI is 0.03 whereas for DG FDSOI it is 0.06. So, it is concluded that DG FDSOI reduced the SCEs upto some level.

All these features should make the proposed DG FDSOI a prime candidate for future CMOS chips.

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