INTERFACING SOLAR PV AND BATTERY STORAGE SYSTEM TO GRID USING THREE LEVEL NPC INVERTER WITH ADVANCED CONTROL SCHEME

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ABSTRACT

A new configuration of a three level neutral point clamped inverter that can integrates solar photovoltaic with battery storage in a grid connected system is proposed in this paper. The proposed system has capability of generating correct Ac voltage under unbalanced DC bus voltage conditions. This paper present the design philosophy of proposed configuration and the theoretical frame work of proposed modulating technique. The control scheme has capability of control the power delivery between the solar PV, battery, and grid, it simultaneously provides maximum power point tracking (MPPT) operation for the solar PV. The usefulness of the proposed methodology is investigated by the simulation of several scenarios, including battery charging and discharging with different levels of solar irradiation.

Keywords: Battery Storage System, Solar Photovoltaic, Space Vector Pulse Width Modulation, Three- Level NPC Inverter.

I. INTRODUCTION

Nowadays demand for power throughout the world increases and these demands cannot meet by conventional sources (like thermal and hydro generation) because of limited availability of coal and water. Hence entire world foot forward to the renewable energy sources like wind and solar energy they never going to be vanish, and these are the most promising alternatives to replace conventional energy sources [1], [2]. But effective utilization of renewable sources and for getting maximum power output requires fast acting power electronic converters [3].

For three-phase applications, two types of power electronic configurations are commonly used to transfer power from the renewable energy resource to the grid: 1) single-stage and 2) double-stage conversion. In the double-stage conversion for a PV system, the first stage is usually a dc/dc converter and the second stage is a dc/ac inverter. In first stage the DC-DC converter provides maximum power tracking from PV module and also produces appropriate DC voltage for stage-2 inversion. In stage-2 (inversion stage) inverter produces 3-ø sinusoidal voltages or currents and it transfers power to load connected or to the grid.

In the case of single-stage connection, only one converter is desired to fulfill the double-stage functions, and hence the system will have a lower cost and higher efficiency, however, a more complex control method will be

required. For industrial high power applications need a 3-ø system, single stage PV energy systems by using a voltage-source converter (VSC) for power conversion [4], [5].

Because of unpredictable and fluctuating nature of solar PV and wind energy systems the output of these systems not constant at terminal ends to overcome such difficulty a battery storage system is employed. This also can boost the flexibility of power system control and increase the overall availability of the system [2]. Usually, a converter is essential to control the charging and discharging of the battery storage system and another converter is required for dc/ac power conversion; thus, a three phase PV system connected to battery storage will require two converters. This paper is concerned with the design and study of a grid-connected three-phase solar PV system integrated with battery storage using only one three-level NPC converter having the capability of MPPT and ac-side current control, and also the ability of controlling the battery charging and discharging. All these will result the cost of conversion decreases, efficiency goes up and flexibility of power flow control increase. The remainder of the paper is ordered as follows. Section-2 describes the structure of a three-level inverter and associated capacitor voltages. Section-3 presents the proposed topology to integrate solar PV and battery storage and its associated control. Section-4 describes the simulation and validation of the proposed topology and associated control system. Section-5 concludes the paper.

II. THREE-LEVEL INVERTER CONFIGURATION AND ITS CAPACITOR VOLTAGE CONSIDERATIONS

2.1 Three-Level Inverter

The three level inverter was first introduced in 1981 [1], [4], they gets more popular in the areas such as FACT, renewable energy systems, STATCOM, HVDC, PWM rectifiers and more, The structure of three level Neutral point clamped inverter shown in figure 1(a). It has three bridge legs and each leg having four switches. "Three-level" means that each bridge leg, A, B and C can have three different voltage states ($^{+}V_{dc}/_{2}$,0, $^{-}V_{dc}/_{2}$) with respect to DC bus neutral. Switches 1 & 3 and 2&4on each leg are complementary, which means that when switch 1 is on, switch 3 is off and vice versa. The combination of states for the bridge legs give the space vectors plotted in fig.1(b) Space vector 210 means that bridge leg A is in state 2, leg B in state 1 and leg C in state 0. Some of the switching states give the same space vector as is seen for the inner vectors shown in fig.1 (b).

There are three main methods established to control the behavior of the fundamental voltage generated by the three-level inverter to the load. These methods are as follows: 1) carrier-based PWM; 2) space vector pulse width modulation (SVPWM); and 3) selective harmonic elimination (SHE) [8]. This paper deals with SVPWM.

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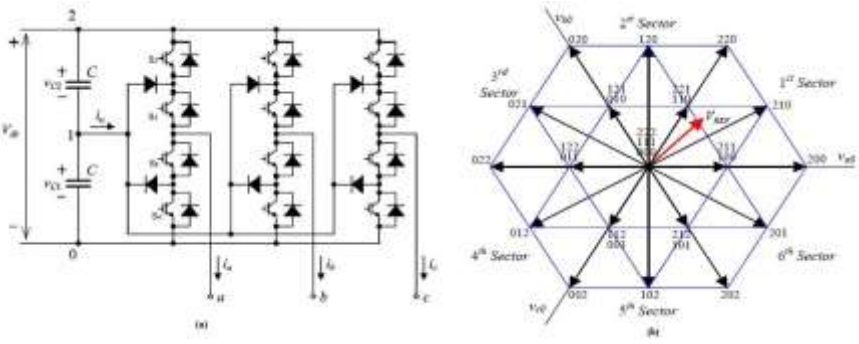

Fig. 1 (a) Typical structure of three-level inverter (b) three-level inverter space vector diagram for balanced dc-link capacitors [1]

The converter has two capacitors in the dc side to produce the three-level ac-side phase voltages. Normally, the capacitor voltages are assumed to be balanced, because unbalance capacitor voltages can affect the ac side voltages and can produce unexpected behavior on system parameters such as even-harmonic injection and power ripple [4], [6]. Several papers have discussed methods of balancing these capacitor voltages in various applications [5]-[9].

2.2 Balanced Capacitors Voltage

Various strategies have been proposed to balance the capacitor voltages using modulation algorithms such as sinusoidal carrier based PWM (SPWM) or space vector pulse width modulation (SVPWM) [4]. In SPWM applications, most of the strategies are based on injecting the appropriate zero-sequence signal into the modulation signals to balance the dc-link capacitors [10], [11]. In SVPWM applications, a better understanding of the effects of the switching options on the capacitor voltages in the vector space has resulted in many strategies proposed to balance capacitors voltages in the three-level NPC inverter. These include capacitor balancing using conventional SVPWM, virtual SVPWM (VSVPWM) and their combination [12], [13].

Ideally, the inverter must be able to generate the voltage output instantaneously, following the reference vector($\bar{v}_{ref}$), generated by the control system. However, because of the limitation of the switches in the inverter, it is not possible to guarantee that any requested vector can be generated; as a matter of fact, only a limited number of vectors (27 vectors for three-level inverter) can be generated. To overcome such difficulties, in any space vector modulation (SVM) scheme such as SVPWM and VSVPWM, the reference vector v_{ref} is generated by selecting the appropriate available vectors in each time frame in such a way that the average of the applied vectors must be equal to the reference vector.

$$T_S V_{ref} = \sum_{i=1}^{n} T_i V_i$$

$$T_S = \sum_{i=1}^{n} T_i \qquad (1)$$

Where *Ts* is the time frame and preferred to be as short as possible. It can be considered as a control update period where an average vector will be mathematically generated during this time duration. *Ti* is the corresponding time segment for selected inverter vector V_i and *n* is the number of applied vectors.

Generally, the reference vector is generated by three different vector (n = 3), and (1) can be converted to three different equation with three variables *T*1, *T*2, and *T*3 to be calculated. Several vector PWM techniques presented in [6], [7], [9]–[11], and [13] apply similar technique of timing calculation. Fig. 1(b) shows the space vector diagram of a three-level inverter for balanced dc-link capacitors [7]. It is made up of 27 switching states, from which 19 different voltage vectors can be selected. The number associated with each vector in Fig. 1(b) represents the switching state of the inverter phases respectively. The voltage vectors can be categorized into five groups, in relation to their amplitudes and their effects on different capacitor voltages from the view of the inverter ac side. They are six long vectors (200, 220, 020, 022, 002, and 202), three zero vectors (000, 111, and 222), six medium vectors (210, 120, 021, 012, 102, and 201), six upper short vectors (211, 221, 121, 122, 112, and 212), and six lower short vectors (100, 110, 010, 011, 001, and 101).

For generating $\bar{v}_{ref}$, when one of the selections (V_i), is a short vector, then there are two choices that can be made which can produce exactly the same effect on the ac side of the inverter in the three wire connection (if

voltages are balanced). For example, the short vector "211" will have the same effect as "100" on the ac side of the inverter. However, this choice will have different effect on the dc side, as it will cause a different dc capacitor to be chosen for the transfer of power from or to the ac side, and a different capacitor will be charged or discharged depending on the switching states and the direction of the ac side current. For example, Fig. 2 shows the connection of the capacitors when "100"or "211" is selected, demonstrating how different capacitors are involved in the transfer of power.

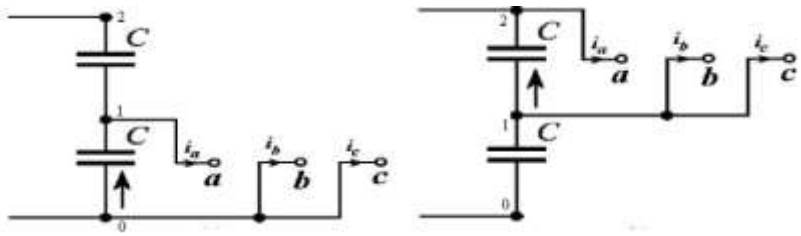

Fig. 2 Equivalent Circuit and Capacitor Current with Two Different Shot Vectors (100) and (211)

In three level inverter applications the capacitor voltage balance is achieved through proper selection of short vectors. In order to produce AC side wave forms the vector diagram shown in fig. 1(b) is used (here the DC side capacitor voltages are assumed balanced). Fig. 1(b) is used to determine the three nearest vectors which are used to produce reference vector, and their corresponding timing are calculated by expression given in (1). If some of the cases like transients and unexpected operations the capacitor voltages are unbalance even though control system tries to balance capacitor voltages, on those cases the AC side wave forms have even harmonics and power ripples.

However, in some applications, the requirement of having balanced capacitor voltages may be too restrictive. The method proposed in this paper is based on the choice of having balance or unbalanced capacitor voltages. In such applications, it is important to be able to generate an accurate reference vector based on expression (1), irrespective of whether the capacitor voltages are balanced or not, to achieve the desired objectives of the system.

2.3 Unbalanced Capacitor Voltages

In the vector diagram shown in Fig. 1(b), capacitor voltage unbalance causes the short and medium vectors to have different magnitudes and angles compared to the case when the capacitor voltages are balanced. Fig. 3 shows the differences between two cases as highlighted in the first sector of the hexogen in Fig. 1(b) for $V_{C1} < V_{C2}$. The calculation of vector in each switching state is described in section 2.4.

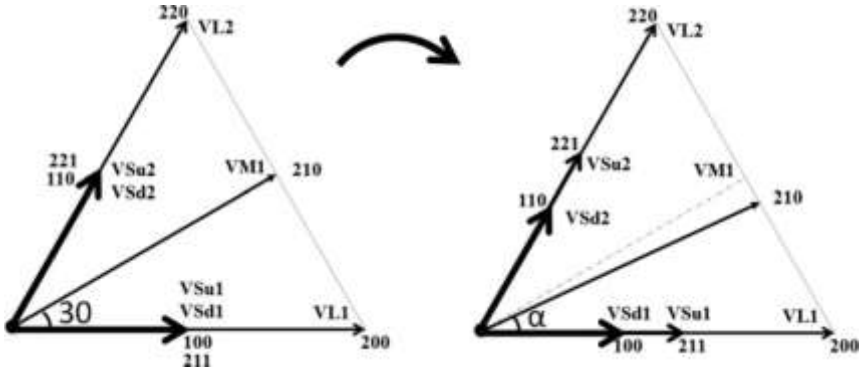

Fig. 3 Vector Diagram in the First Sector of Fig. 1(B) Showing the Change of the Vectors Using Balanced Dc and Unbalanced Dc Assuming ($V_{c1}<V_{c2}$)

2.4 Calculation of Vector Magnitude and Phase for Each Switching State

The requested Vector related to the switching state $\vec{V}_I$ can be calculated as follows: [1]

$$\vec{V}_I = \frac{2}{3}\left(V_{an} + \vec{a}V_{bn} + \vec{a}^2 V_{cn}\right) \quad (2)$$

Where $a = e^{j\left(\frac{2\Pi}{3}\right)}$ V_{aN}, V_{bN} and V_{cN} are the voltage values of each phase with reference to "*N*" (where *N* is the neutral point on DC bus side) . Assuming that the length of the long vectors $\frac{2}{3}V_{dc}$ is 1 unit and the voltage of capacitor *C*1, $V_{c1} = hV_{dc}$, for $0 \le h \le 1$, then the vectors in the first sector can be calculated using (2) and the results are given in equations (3)–(9).

$$\left.\begin{array}{l}
\vec{V}_{sd1} = h \\
\vec{V}_{su1} = 1-h \\
\vec{V}_{l1} = 1 \\
\vec{V}_{l2} = \frac{1}{2} + \frac{\sqrt{3}}{2}j = \mathrm{cis}(60) \\
V_{sd2} = h * \mathrm{cis}(60) \\
\vec{V}_{su2} = (1-h)(\mathrm{cis}(60)) \\
\vec{V}_{m1} = \left(1-\frac{h}{2}\right) + h\frac{\sqrt{3}}{2}
\end{array}\right\} \quad \text{eq. (3) - (9)}$$

The vectors in the other sectors can be calculated similarly. Equations (3)–(9) show that the magnitudes and the angles of the vectors can change depending on the value of the capacitor voltages. For example, when $h = 0.5$, then the two capacitor voltages are the same and the two short vectors are the same $\vec{V}_{sd1} = \vec{V}_{su1}$. However, when the two capacitor voltages are different, the vectors will have different magnitudes. Since the short vectors are now different in magnitude, the choice of these short vectors will now have a different effect on both the dc and ac side. Traditionally, each pair of short vectors is considered to be redundant, as the selection of any of the short vectors at any instance will have the same effect on the ac side. However, when the two capacitor voltages are different, the short vectors cannot be considered to be redundant any more. Thus, when $h \neq 0.5$, each different short vector needs different timing to generate the requested vector based on (1).

2.5 Selection of Vectors to Generate V_{ref} Vector and Their Effects on AC and DC Side of Inverter

To generate a reference vector based on (1), different combinations can be implemented. Fig. 4 shows different possible vector selections to generate a reference vector V_{ref} in the first sector based on the selections of different short vectors. For example, to generate V_{ref} based on Fig. 4(a), one of following combinations can be selected with proper timing based on (1). The combinations are: (221–210–100), (221–220–100), (221– 200–100), (221–200–Zero), (000–220–Zero), (220–200–Zero), where "Zero" can be "000" or "111" or "222". This demonstrates that there is flexibility in choosing the correct vector selections. Although all of these selections with suitable timing can generate the same reference vector, they have different impacts on the dc and ac side of the inverter in their instantaneous behavior.

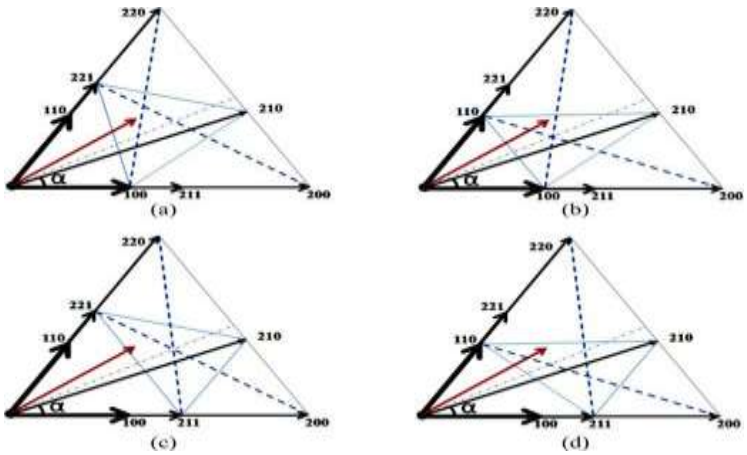

Fig. 4 different possible vector selection ideas [1]

2.5.1 AC Side Behavior

To investigate the ac-side behavior, the accuracy of the generated voltage must be examined. As far as the AC is concerned, ideally the requested voltage $\vec{v}(t)$ should be exactly and simultaneously generated in the three phases of the inverter to have the correct instantaneous current in the ac side of the system. However, because of the limitation of the inverter to generate the exact value of the requested voltage in each phase, in the short time T_s, only the average value of the requested vector $\vec{v}(t)$ for the specified time window of T_s can be produced.

To investigate the continuous time behavior of the ac-side voltages, the error vector $\vec{e}(t)$ can be calculated in order to determine how far the generated voltage deviates from the requested vector as follows [1]:

$$\vec{e}(t)=\vec{V}(t)-\vec{V}_{apl}(t) \tag{10}$$

$$E(t)\triangleq\left|\int_0^t \vec{e}(t)\,dt\right| \tag{11}$$

Where $\vec{V}_{apl}(t)$ is the applied vector at the time "*t*". This error can result in harmonic current across the impedance connected between the inverter and the grid. If this impedance is an inductor then the ripple in the inductors current $\vec{I}_{rL}$ can be expressed as

$$\vec{I}_{rL}=\frac{1}{L}\int_0^t \vec{e}(t)\,dt \tag{12}$$

Where $\vec{e}(t)$ is defined as

$$\vec{e}(t)\triangleq L\frac{d\vec{I}_{rL}}{dt} \tag{13}$$

To derive (13), it is assumed that the requested vector $\vec{v}(t)$ will generate sinusoidal current in the inductor, which is normally acceptable in the continuous time behavior of the system. Based on (11) and (12), the absolute value of error $E(t)$ is directly related to the magnitude of the inductors current ripple. Although based on (1) and (11), $E(T_s) = 0$ or the sum of errors during the period T_s is zero; but to reduce the magnitude of high frequency ripples, it is important to minimize the error at each time instant. To achieve this, the three nearest vectors (TNV) are usually used. For example, in Fig. 4(a), to generate the requested vector $\vec{v}(t)$ in the TNV method, the group (221, 210, 100, or 211) appears to be the best three nearest vectors to be chosen.

Also, to reduce $E(t)$, a smart timing algorithm for each vector in the TNV method has been proposed, such as dividing the time to apply each vector into two or more shorter times. However, this will have the effect of increasing switching losses. Dividing by two is common, acceptable solution. Moreover, reducing T_s will reduce the error $E(t)$ while improving the accuracy of the requested vector generated by the control system. According to the basic rule of digital control, accuracy of the requested vector calculation can be improved by reduction of the sampling time and the vector calculation time.

2.5.2 DC Side Behavior

As far as the dc side is concerned, different vectors have different effects on the capacitor voltages which depends on the sum of the incoming currents from the dc side and the inverter side. The currents coming from the inverter are related to the inverter switching and the ac side of inverter currents which can be directly affected by the implemented vectors in the inverter. Selecting different vectors will transfer ac-side currents and power differently to the capacitors as discussed in Section 2.2.

The instantaneous power transmitted to the dc side of the inverter from the ac side can be calculated as follows [1]:

$$p(t) = v_{Ia}.i_a + v_{Ib}.i_b + v_{Ic}.i_c \quad (14)$$

Where v_{Ia}, v_{Ib} , and v_{Ic} are the ac-side inverter instantaneous voltages with reference to the "N" point, and i_a, i_b, i_c are inverter currents. For example, in the first sector of the vector diagram shown in Fig. 3, $p(t)$ for the short vectors can be expressed by the following equations:

$$\begin{cases} p_{211}(t) = (1-h)V_{dc} * i_a \\ p_{100}(t) = hV_{dc} * (-i_a) \end{cases} \quad (15)$$

$$\begin{cases} p_{221}(t) = (1-h)V_{dc} * (-i_c) \\ p_{100}(t) = hV_{dc} * (i_c) \end{cases} \quad (16)$$

Ignoring the dc-side system behavior, selecting the upper short vectors, "211" and "221," will affect the upper capacitor voltage, and selecting the lower short vectors, "100" and "110," will affect the lower capacitor voltage. For example, when $i_a > 0$, if vector "211" is selected, it will charge the upper capacitor without any effect on the lower capacitor voltage and if vector 100 is selected, it will discharge the lower capacitor without having any effect on the upper capacitor voltage. By using (15) and (16), the rate of charging and discharging and their dependency on h and V_{dc} values and inverter currents can also be observed. However, for accurate investigations, the dc side system behavior needs to be considered in the control of charging and discharging rates of the capacitor voltages.

III. PROPOSED TOPOLOGY TO INTEGRATE SOLAR PV AND BATTERY STORAGE

Based on the discussions in Sections 1 and 2, two new configurations of a three-level inverter to integrate battery storage and solar PV shown in fig. 5 are proposed, where no extra converter is required to connect the battery storage to the grid connected PV system. These can reduce the cost and improve the overall efficiency of the whole system particularly for medium and high power applications. fig. 5 Proposed configurations for integrating solar PV and battery storage: (a) basic configuration; (b) improved configuration. fig. 5(a) shows the

diagram of the basic configuration. In the proposed system, power can be transferred to the grid from the renewable energy source while allowing charging and discharging of the battery storage system as requested by the control system. The proposed system will be able to control the sum of the capacitor voltages (V_{C1} + V_{C2} = V_{dc}) to achieve the MPPT condition and at the same time will be able to control independently the lower capacitor voltage (V_{C1}) that can be used to control the charging and discharging of the battery storage system. Further, the output of the inverter can still have the correct voltage waveform with low total harmonic distortion (THD) current in the ac side even under unbalanced capacitor voltages in the dc side of the inverter.

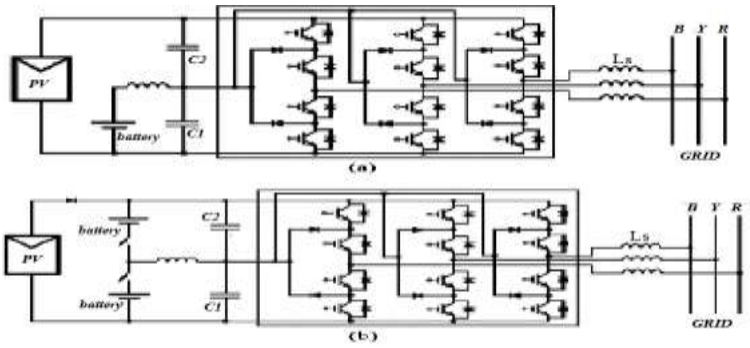

Fig. 5 Proposed Configurations For Integrating Solar PV And Battery Storage: (a) Basic Configuration; (b) Improved Configuration [1].

Although this configuration can operate under most conditions, however when the solar PV does not produce any power, the system cannot work properly with just one battery. fig. 5(b) shows the improved configuration where two batteries are now connected across two capacitors through two relays. When one of the relays is closed and the other relay is open, the configuration in fig. 5(b) is similar to that in fig. 5(a) which can charge or discharge the battery storage while the renewable energy source can generate power. However, when the renewable energy is unavailable, both relays can be closed allowing the dc bus to transfer or absorb active and reactive power to or from the grid. It should be noted that these relays are selected to be ON or OFF as required; there is no PWM control requirement. This also provides flexibility in managing which of the two batteries is to be charged when power is available from the renewable energy source or from the grid. When one of the batteries is fully charged, the relay connected to this battery can be opened while closing the relay on the other battery to charge. Special consideration needs to be made to ensure that current through the inductor L_{batt} must be zero prior to opening any of these relays to avoid disrupting the inductor current and also to avoid damaging the relay. In fig. 5(b), three different relay configurations can be obtained:

1) When the top relay is closed; 2) when the bottom relay is closed; and 3) when both relays are closed.

3.1 Control Scheme

The requested active and reactive power generation by the inverter to be transferred to the grid will be determined by the network supervisory block. This will be achieved based on the available PV generation, the grid data, and the current battery variables. Figure 6 shows the functional block diagram of control scheme of "integration of solar PV and battery storage system to grid through NPC three-level inverter". Most of the blocks already discussed in previous sections, the MPPT block is used to get maximum power from solar PV, most of the papers explains MPPT algorithms [14],[15].

Based on the requested active ($p*$) and reactive power ($q*$), and the grid voltage in the dq-axis, v_{sd} and v_{sq} , the requested inverter current in the dq-axis, i_d and i_q can be obtained using (17):

$$\left.\begin{aligned} p^* &= V_{sd} I_d + V_{sq} I_q \\ q^* &= V_{sq} I_d + V_{sd} I_q \end{aligned}\right\}$$
$$\left.\begin{aligned} i_d^* &= \frac{p^* v_{sd} - q^* v_{sq}}{v_{sd}^2 + v_{sq}^2} \\ i_q^* &= \frac{q^* v_{sd} - p^* v_{sq}}{v_{sd}^2 + v_{sq}^2} \end{aligned}\right\} \qquad (17)$$

After evaluating the requested reference voltage vector, the appropriate sector in the vector diagram can be determined [18]. To determine which short vectors are to be selected the relative errors of capacitor voltages given in (18), [1].

$$e_{v_{c1}} = \frac{v_{c1}^* - v_{c1}}{v_{c1}}$$
$$e_{v_{c2}} = \frac{v_{c2}^* - v_{c2}}{v_{c2}} \qquad (18)$$

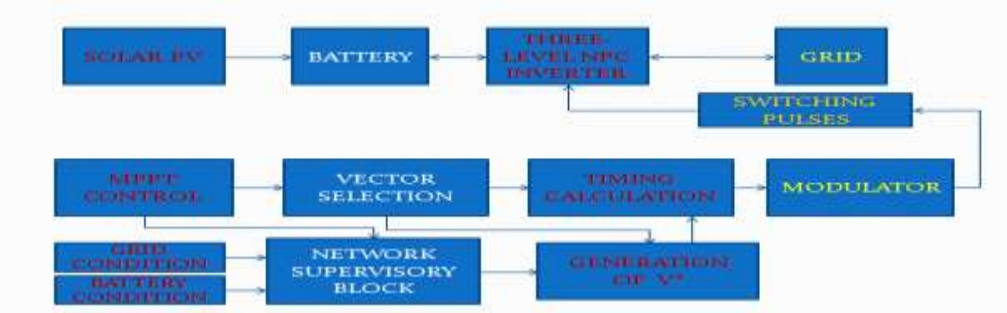

Fig. 6 Functional Block Diagram of Proposed System

where v_{c1} and v_{c2} are the desired capacitor voltages, and V_{C1} and V_{C2} are the actual capacitor voltages for capacitor C_1 and C_2 , respectively.

IV. SIMULATION AND VALIDATION OF PROPOSED TOPOLOGY

Simulations have been carried out using MATLAB/Simulink to verify the effectiveness of the proposed topology and control system. An *LCL* filter is used to connect the inverter to the grid. Fig. 7 shows the block diagram of the simulated system. The mathematical model of each of the PV units is given in [16] and used in the simulation. The values used for simulation are given in table 1.

Table 1 Parameters of the Simulated System

V_{bat}	V_s(line)	L_{bat}	$_{C1,C2}$	L_1	L_s	r_f	C_f
60v	50v	5mH	1000uf	500uh	90uh0	3Ω	14uF

It is assumed that the solar irradiation will produce I_{sc} = 7.03A (short circuit current of solar module at given solar irradiation), V_{dc}^* PV module voltage is 102V to achieve MP from PV that can generate 777.3W of electrical power. Fig. 8 show the simulated result, 8(a) shows the phase to phase inverter voltage, 8(b) shows the

inverter phase voltage with respect to load neutral, 8(c) shows voltage of inverter with respect to midpoint of DC bus, 8(d) shows load current, 8(e) shows active power injected to the grid.

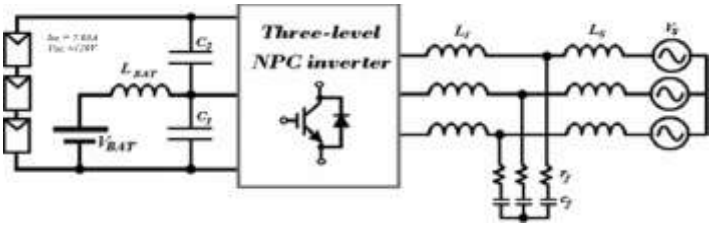

Fig. 7 Block Diagram of the Simulated System

4.1 Simulated Result

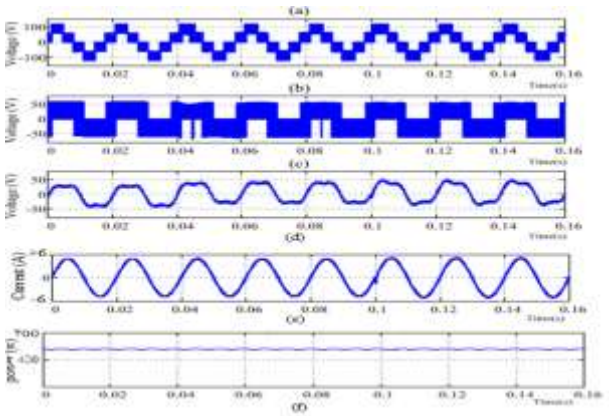

Fig. 8 Simulated Results

V. CONCLUSION

A novel topology for a three-level NPC voltage source inverter that can integrate both renewable energy and battery storage on the dc side of the inverter has been presented. A theoretical framework of a novel extended unbalance three-level vector modulation technique that can generate the correct ac voltage under unbalanced dc voltage conditions has been proposed. A new control algorithm for the proposed system has also been presented in order to control power flow between solar PV, battery, and grid system, while MPPT operation for the solar PV is achieved simultaneously. The effectiveness of the proposed topology and control algorithm was tested using simulations and results are presented. The results demonstrate that the proposed system is able to control ac-side current, and battery charging and discharging currents at different levels of solar irradiation.

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