DESİGN AND ANALYSİS OF FULL ADDER CİRCUİT USİNG NANOTECHNOLOGY BASED QUANTUM DOT CELLULAR AUTOMATA (QCA)

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ABSTRACT

Recent experiments in the field of VLSI designing and Nanotechnology have demonstrated a working cell suitable for implementing the Quantum-dot Cellular Automata (QCA). QCA is a transistor less computational model which is expected to provide high density nanotechnology implementations of various CMOS circuits. QCA has been constrained by the problem of power loss. QCA adder with comparatively less number of cells and area has been proposed in this paper. This paper also demonstrates a reversible logic synthesis for full adder which gives a superior solution in terms of complexity, area and latency. The new proposed hybrid method reduces cell counts and area and uses conventional form of QCA cells.QCA implementation provides efficient design methodology for faster speed, smaller size and low power consumption when it compared to technology imposed by transistors.QCA provides ability to quickly layout a QCA design by providing an extensive set of CAD tools.

Keywords: Combinational Circuits, Majority Gates, Quantum-Dot Cellular Automata (QCA), Quantum Cost, Reversible Logic, Latency.

I. INTRODUCTİON

Prior studies suggest that design complexity can be substantially influenced by the majority gate count. The number of majority gates also indirectly determines the cell count due to QCA wires in a design. It is therefore of interest to design methods that involve systematic reduction of majority gates and inverters [6-7]. To the best of our knowledge, there has been no prior work on deriving simplified expressions involving majority gates and inverters for various types of adders.QCAs are never free from fabrication imperfections. The influence of imperfections stem from:

1) Changes of intercellular distance
2) Changes of the height of the inter dot barriers
3) Presence of stray charges

The proposed implementation uses the advantage of the reversible logic. Minimization of the number of reversible gates, quantum cost and garbage outputs is the focus of research of this paper. In Section II, basic logic gates are discussed in brief. In Section III, some of the previous adder designed are discussed using i-corner method and without cross connection. Conclusions are presented in last Section.

II. LOGIC GATES

Logic gates are required to build arithmetic circuits. In QCA, inverters and three-input majority gates serve as the fundamental gates.

2.1 QCA Wıres

In a QCA wire, the propagation of binary signal takes place from input to output due to the electrostatic interactions between cells. Since the polarization of each cell tends to align with that of its neighbors, a linear arrangement of standard cells is used to transmit binary information from one point to another.. A QCA wire is shown in Figure 1.

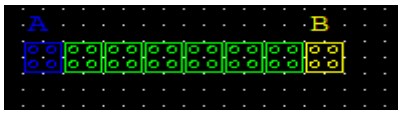


Fig.1.QCA wire

2.2. Majority Gate

The governing equation for the majority gate is M (a; b; c) = ab+ bc + ca. Fig. 1 shows the gate symbols and their layouts. Two input AND and OR gates can be implemented with 3 input majority gates by setting one input to a constant. With ANDs, ORs, and inverters, any logic function can be realized.

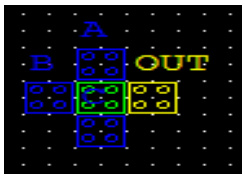


Fig.2 Majority Gate

2.3 .QCA Inverter

QCA Inverter can be implemented in position QCA cells to invert the output from input logic level.In this ,the input is split into two and finally it impinges at the output to form the inverted input.

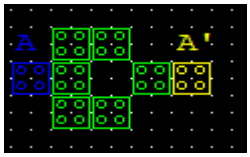
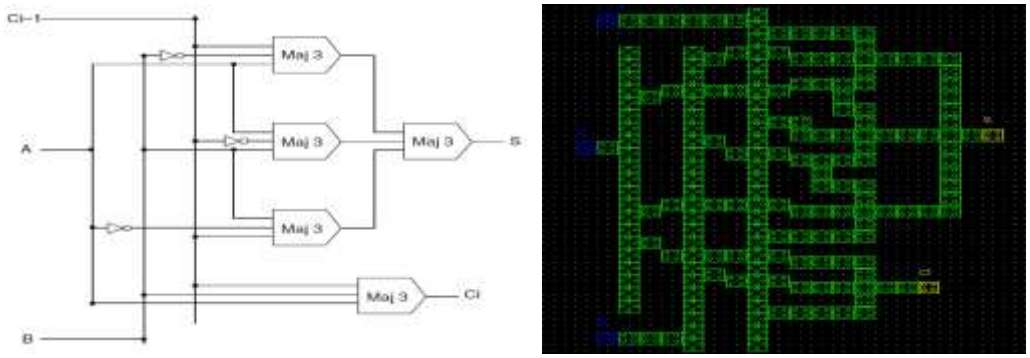


Fig.2 Inverter

III. PREVIOUS WORK

3.1. QCA Adders Implementatıon Usıng I-Corner

Majority gates a basic building block of QCA circuits. The number of majority gates used depends on the circuit to be implemented using QCA. Most of the circuits uses three input or five-input majority gates in designing QCA circuits.Five 3-input majority gates and three inverters are used to implement QCA Full-Adder l-corner using and its schematic and layout is shown in Fig.2.The adder designed by using minimal inverter proposed by Lusth and Jackson having corner turns is introduced to remove the meta-stability problem and to overcome the limitations of Quasi adiabatic switching .It is used for providing the asymmetric spacing.The adder designed by using minimal inverter work correctly for some separation distances The adder performed significantly better ,tolerating separation distances up to 65 nm with a peak **A** of 0.166 mV at a separation distance of 50 nm.



(a) **(b)**

Fig.3 One bit QCA Full-Adder. (a) Schematic of the first QCA Full-Adder (b) Layout of this Full-Adder

3.2. QCA Adder Implementatıon Wıth Three-Input Majorıty Gates

A full adder is a combinational circuit which is used for addition of three one bit binary inputs and produces two one bit binary outputs. In our proposed design, A0 and B0 are the two operands and C0 is the output carried from the less significant stage. The circuit produces two outputs represented as sum and carry. Expression of full adder:

$$\text{Sum} = a'b'c + a'bc' + ab'c' + abc$$

$$= \text{majority}[\ \text{majority}(a,b,c)',\ \text{majority}(a,b,c'),c]$$

$$\text{Carry} = ab+bc+ca = \text{majority}(a,b,c)$$

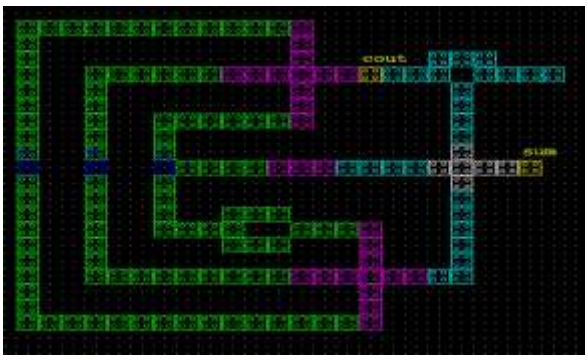


Fig.4 The QCA İmplementation of the Previous Adder

The simulation of the circuits was done using QCA Designer tool . In QCA Designer, cells are assumed to have width and height of 18nm. The quantum dots are also assumed to be 5nm in diameter and the cells are placed on a grid with center-to-center distance of 20nm.

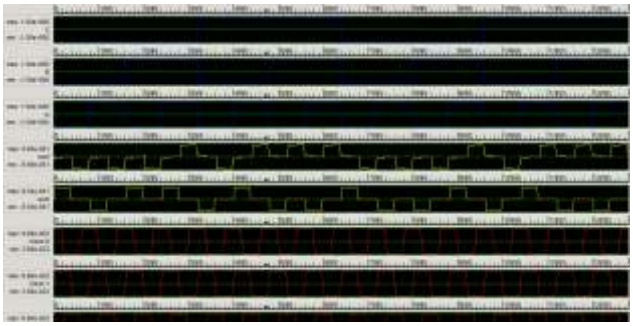


Fig.5 Simulated Waveforms of Adder Circuit Using Reversible 3MV Gates

IV. PROPOSED WORK

In this section, the reversible majority gate is applied to implement a QCA adder. [4] The full adder circuit's output is given by the following equations:

$$Sum=A (+) B (+) Cin$$

$$Cout= (A (+) B) Cin (+) AB$$

Where (+) is exclusive OR

This paper presents a novel adder using QCA. In non-reversible gates there is a definite amount of power loss involved.The following demonstrates that the proposed full adder gate is superior to the existing counterparts in terms of hardware complexity, quantum costs, garbage outputs and constant inputs. The reversible adder gate takes three inputs say A0, B0 and C0 and produces two outputs SUM and CARRY out of which one output SUM is the XOR of three inputs A, B and C. In order to implement this gate in QCA, 3- three input majority gates and two inverters is required as shown in Fig. 6.

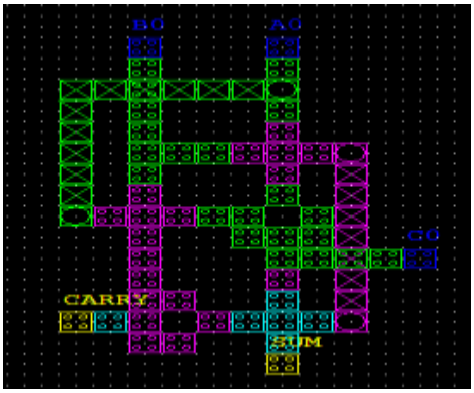


Fig.6.QCA İmplementation of Proposed Full Adder Design

V. SIMULATION

With QCA Designer ver.2.0.3, the circuit functionality is verified. QCA Designer is the most popular simulation tool for semiconductor QCA circuit design. QCA Designer is capable of simulating complex QCA circuits on most standard platforms. The current version of QCA Designer has three different simulation engines included. The QCA Designer 2.0.3, there are two simulation engines: the bi- stable engine and coherence engine.

5.1. Setup Parameters

In QCA Designer, cells are assumed to have following parameters as shown in table below

Table 1: Set Up Parameter

Width and height	18nm
Diameter of quantum dots	5nm
Center to center distance	20nm
Scale for all factors	1
Clock high	9.8e-22j
Clock low	3.8e-23j
Upper threshold	0.5000
Lower threshold	-0.5000
No. of samples	12000

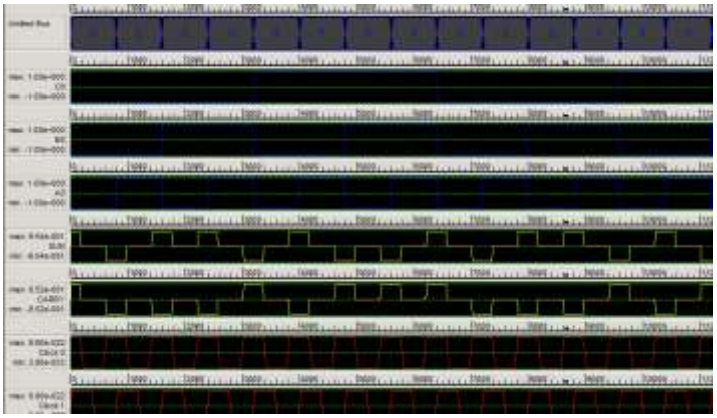


Fig.7. Simulated Waveforms of Proposed Adder Circuit

VI. RESULTS

The simulation of the circuits was done using QCA Designer tool . With QCA Designer ver.2.0.1, the previously proposed logical structure functionality was verified. This version of QCAD is used to implement the l- corner designs of inverters. In QCA Designer, cells are assumed to have width and height of 18nm. The quantum dots are also assumed to be 5nm in diameter and the cells are placed on a grid with center-to-center distance of 20nm

Designs	Gate count	Area(um2)	complexity	latency
I	5 MG 3 inverter	0.20	192	>1 clock
II	3 MG 2 inverter	0.25	124	>1 clock
proposed	3 MG 2 inverter	0.15	81	<clock

VII. CONCLUSION

The proposed designs are a solution for implementations of QCA based circuits using minimum number of QCA cells, lesser clock delays and reduced area. This paper has demonstrated the design of improved QCA adder structures, which will be useful as an efficient building block for larger arithmetic units. The simulation results of proposed (full) adder circuit have been verified using QCA Designer. This novel unit has been found to have less practical latency and better throughput compared to the best corresponding cases found in the literature, the circuit area is found to be reduced to a fraction of the previous noise rejecting implementations. One aim of this paper is to design simple QCA structures with available basic gates with capable versatility and minimum garbage outputs susceptibility. In addition, results are verified by the truth table

VIII. THE FUTURE WORK

This paper has demonstrated the design of improved QCA adder circuits, which will beuseful as an efficient building block for larger arithmetic logic units (ALU) in future. The proposed architectural structures can be applied not only to general purpose processing, but to special purpose processing as well. The possibilities of applying the QCA technology to special purpose processing (such as digital signal processors) can also be explored.

REFERENCES

[1]. P. D. Tougaw and C. S Lent, "Logical devices implemented using quantum cellular automata". Appl. Phys.Vol75, pp. 1818-1825, 1818(1994).

[2]. W. Wang, K. Walus, and G. A. Jullien, "performance comparison of Quantum-dot cellular automata adders", 3rd IEEE Conference on Nanotechnology, vol. 3, pp. 461–464, (2003).

[3]. R. Zhang, K. Walus, W. Wang, and G. A. Jullien, "A method of majority logic reduction for quantum cellular automata," IEEE Trans. Nanotechnol.,vol. 3, no. 4, pp. 443–450, Dec. 2004.

[4]. J. Huang, M. Momenzadeh, M. B. Tahoori, and F. Lombardi, "Design and characterization of an And-Or-Inverter (AOI) gate for QCA implementation", Proc. Great Lakes Symp, VLSI (GLSVLSI), pp. 426–429, Boston(2004).

[5]. H. Cho and Earl E. Swartzlander, Jr., "Modular Design of Conditional Sum Adders Using Quantum-dot Cellular Automata", Nanotechnology, 2006. IEEE-NANO 2006. Sixth IEEE Conference on (Volume:1) pp. 363 – 366 June 2006.

[6]. H. Zhi, Q. Zhang, S. Haruehanroengra, and W. Wang, "Logic optimization for majority gate based nanoelectronic circuits", International Symposium on Circuits and Systems ISCAS, pp. 1307–1310,2006.

[7]. Stefania Perri, Senior Member, IEEE, Pasquale Corsonel, Member, IEEE, and Giuseppe Cocorullo, Member, IEEE," Design of Efficient Binary Comparators in Quantum-Dot Cellular Automata", IEEE Transaction on Nanotechnology,vol. 13, no.2, Mar 2014.

[8]. A.O. Orlov, I. Amlani, G.H. Bernstein, C.S. Lent, G.L. Snider, "Realization of a Functional Cell for Quantum-Dot Cellular Automata," Science, Vol 277, pp 928-930, 1997