HİGH SPEED LOW POWER ERROR TOLERANT ADDER FOR IMAGE COMPRESSİON

Richa Chaturvedi[1], Dr. Rita Jain[2], Dr. M.K.Gupta[3]

[1]Phd Scholar, AISECT University, Bhopal, Madhya Pradesh, (India)

[2] Professor, Dept of ECE, Lakshmi Narain College of Technology, Bhopal, Madhya Pradesh, (India)

[3] Professor, Dept of ECE,Maulana Azad National İnstitute of Technology, Bhopal, Madhya Pradesh, (India)

ABSTRACT

Low power is an imperative requirement for portable multimedia devices employing various signal processing algorithms and architectures. In most multimedia applications, human beings can gather useful information from slightly erroneous outputs. This paper contributes to better understanding of the behaviour of single-bit full adder cells when lowest power-delay products are essential. Four single-bit full adder cells have been implemented in Cadence tool suit and simulated using 180nm CMOS technology to obtain a comprehensive study of the performance of the cells with respect to time (time-delays) and power consumption (power dissipation). Simulation method used for performance measurements has been carefully devised to achieve as accurate measurements as possible with respect to time delay and power consumption. The method combines the simple measurement technique for obtaining accurate time-delays and power consumption of a cell, and the transistor resizing technique that allows systematically resizing of transistors to achieve minimal power-delay product.

Keywords: DSP application, High Speed,Low Power, Tolerant adder.

I. INTRODUCTION

In applications such as a communication system, the analog signal coming from outside world must first be sampled before we can convert it to digital data at the front end of the system. The digital data is then processed and transmitted in a noisy channel before being converted back to the analog signal at the back end. During this process, errors may occur everywhere. Furthermore, due to the advances in transistor size scaling, the previously insignificant factors such as noise and process variations are becoming important impacts in today's digital IC design [2]. Based on the characteristic of digital VLSI design, some novel concepts and design techniques have been proposed. The concept of error tolerance (ET) has proposed in [3]–[10]. According to the definition, a circuit is error tolerant if: 1) it contains defects that cause internal and external errors and 2) the system that includes this circuit produces acceptable results [3] not accurate but approximate. The "imperfect" result not appealing for the system attribute. However, the need for the error-tolerant circuit [3]–[10] was foretold in the 2003 International Technology Roadmap for Semiconductors (ITRS) [2].

To deal with error-tolerant problems, some truncated adders/multipliers have been reported [11], [12] but are not able to perform well in either its speed, power, area, or accuracy. The "flagged prefixed adder" [11] performs better than the non flagged version with a 1.3% speed enhancement but at the expense of 2% extra silicon area.

As for the "low-error area-efficient fixed-width multipliers" [12], it may have an area improvement of 46.67% but has average error reaching 12.4%. Of course, not all digital systems can engage the error-tolerant concept. In digital systems such as control systems, the correctness of the output signal is extremely important, and this denies the use of the error tolerant circuit. However, for many digital signal processing (DSP) systems that process signals relating to human senses such as hearing,

In this section, we discuss different methodologies for designing approximate adders. We use ripple carry adders (RCAs) and carry select adders CSAs throughout our subsequent discussions in all sections of this paper. Since the Mirror adder MA [13] is one of the widely used economical implementations of an full adder FA [14], we use it as our basis for proposing different approximations of an FA cell.

1.1 Approximation Strategies for the MA

In this section, we explain step-by-step procedures for coming up with various approximate MA cells with fewer transistors. Removal of some series connected transistors will facilitate faster charging/discharging of node capacitances. Moreover, complexity reduction by removal of transistors also aids in reducing the αC term (switched capacitance) in the dynamic power expression $P_{dynamic} = \alpha C V^2_{DD} f$, where activity or average number of switching transitions per unit time and C is the load capacitance being charged/discharged. This directly results in lower power dissipation. Area reduction α is the switching is also achieved by this process. Now, let us discuss the conventional MA implementation followed by the proposed approximations.

1) Conventional MA: Fig. 1 shows the transistor-level schematic of a conventional MA [13], which is a popular way of implementing a FA. It consists of a total of 24 transistors. Since this implementation is not based on complementary S logic, it provides a good opportunity to design an approximate version with removal of selected transistors.

2) Tolerant Adder 1: In order to get an approximate MA with fewer transistors, we start to remove transistors from the conventional schematic one by one. However, we cannot do this in an arbitrary fashion. We need to make sure that any input combination of A,B and C_{in} does not result in short circuits or open circuits in the simplified schematic. Another important criterion is that the resulting simplification should introduce minimal errors in the FA truth table. A judicious selection of transistors to be removed (ensuring no open or short circuits) results in a schematic shown in Fig. 2, which we call approximation 1. Clearly, this schematic as eight fewer transistors compared to the conventional MA schematic. In this case, there is one error in C_{out} and two errors in Sum. A tick mark denotes a match with the corresponding accurate output and a cross denotes an error.

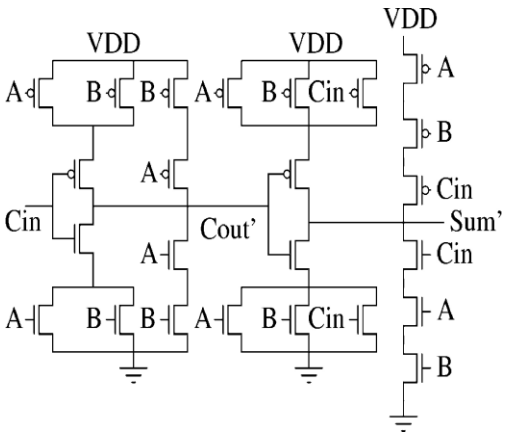

Fig. 1 Conventional Mirror Adder

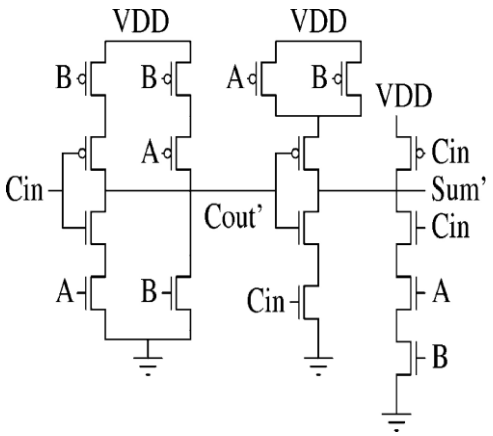

Fig. 2 Tolerant adder Adder 1

3) Tolerant Adder *2:* The truth table of an FA shows that Sum= C_{out} 1 for six out of eight cases, except for the input combinations $A = 0, B = 0, C_{in} = 0$ and $A = 1, B = 1, C_{in} = 1$. Now, in the conventional MA, C_{out} is computed in the first stage. Thus, an easy way to get a simplified schematic is to set Sum= C_{out}. However, we introduce a buffer stage after C_{out} in Fig. 3 to implement the same functionality. The reason for this can be explained as follows. If we set Sum= C_{out} as it is in the conventional MA, the total capacitance at the Sum node would be a combination of four source–drain diffusion and two gate capacitances. This is a considerable increase compared to the conventional case or approximation 1. Such a design would lead to a delay penalty in cases where two or more multi-bit approximate adders are connected in series, which is very common in DSP applications. Fig. 3 shows the schematic obtained using the above approach. We call this approximation 2. Here, Sum has only two errors, while C_{out} is correct for all cases.

4) Tolerant Adder *3:* Further simplification can be obtained by combining approximations 1 and 2. Note that this introduces one error in C_{out} and three errors in Sum. The corresponding simplified schematic is shown in Fig. 4.

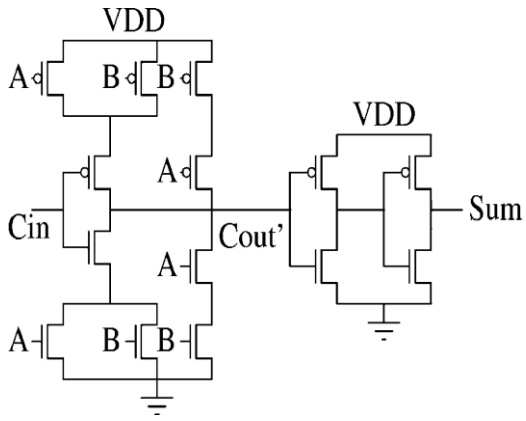

Fig. 3 Tolerant adder Adder 2

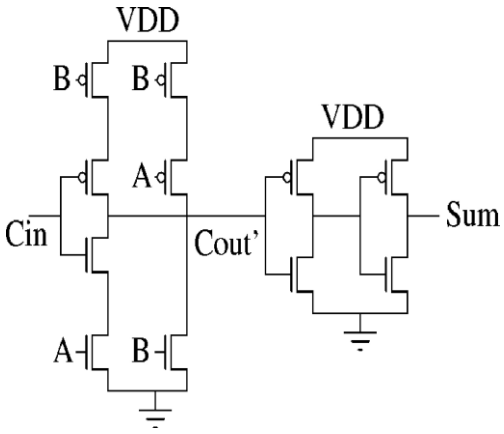

Fig.4 Tolerant adder Adder 3

5) Tolerant Adder *4:* A close observation of the FA truth table shows that $C_{out} = A$ for six out of eight cases. Primarily, $C_{out} = B$ for six out of eight cases. Since A and B are interchangeable, we consider $C_{out} = A$, we propose a fourth approximation where we just use an inverter with input A to calculate C_{out} and Sum is calculated similar to approximation 1. This introduces two errors in C_{out} and three errors in Sum, as shown in Table I. The corresponding simplified schematic is shown in Fig. 5. In all these approximations C_{out} is calculated by using an inverter with C_{out} as input.

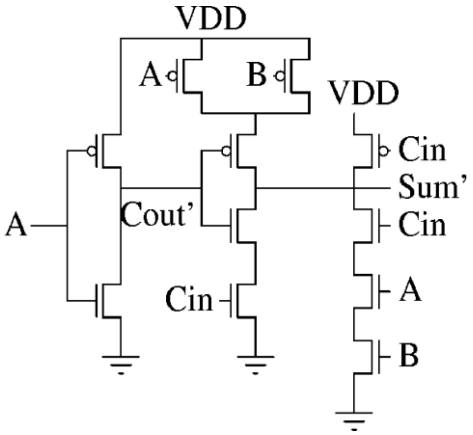

Fig. 5 Tolerant adder Adder 4

III. RESULTS

3.1 Power and Delay Comparison

Power and delay have been calculated in this work and found that power consumption of tolerant adder is very less as compared to the conventional adder. These tolerant adders are approximate but save at least 54% power it can be utilized when no accurate result is required. These tolerant adders are much faster than conventional, speed of such adder are 65% faster than conventional. Comparison of power and delay has been given in table I. The comparative result of power, delay and no. of transistors are shown in fig.6.

Table I Table for Power and Delay of Conventional FA and Tolerant Adder 1–4

	Conventional	Tolerant Adder 1	Tolerant Adder 2	Tolerant Adder 3	Tolerant Adder 4
Power	45.786 pw	30.055 µw	28.335µw	33.60µw	25µw
Delay	5.75µsec	7.8 µsec	4.25 µsec	4.98 µsec	3.75 µsec
No.of Transistor	24	16	14	11	11

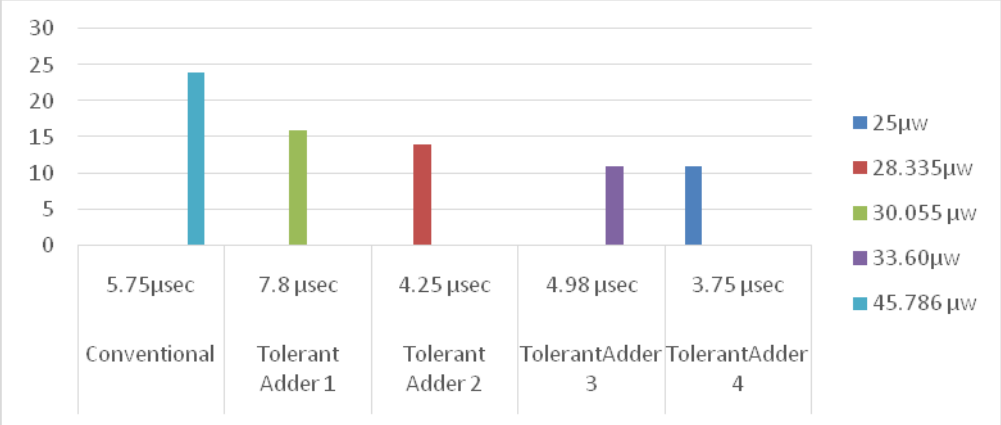

Fig.6 Comparison of Power, Delay and No of Transistors

3.2 Output Quality

The Low Power Digital Image Processing Using Approximate Adder is implemented in VHDL programming language, MATLAB and simulated. It has been synthesized and implemented by cedence 180nm tools. The results are shown in the table II. Power is reduced and image quality is maintained. The output quality of the decoded image after using discrete cosine transform has been evaluated in terms of the well-known metric of peak signal-to-noise ratio (PSNR). The output PSNR for the base case is 31.16 dB. Figure 7 shows the output images for the original and all approximate tolerant adders. It is observed that the blockiness in the second image using Tolerant adder 1. PSNR of the Tolerant adders are listed in table II.

ORGINAL IMAGE

TOLERANT ADDER 1

TOLERANT ADDER 2

TOLERANT ADDER 3

TOLERANT ADDER 4

Fig.7 Compressed İmages using Different Tolerant Adders

TABLE II PSNR and Power Comparison of Tolerant adder

	Mirror Adder	Tolerant adder1	Tolerant adder2	Tolerant adder3	Tolerant adder4
PSNR	32.2	30.12	24.56	34.44	35.56
POWER	160mW	163mW	159mW	156mW	154mW

Comparison of Lena image using different tolerant adders are shown in Figure 8 .

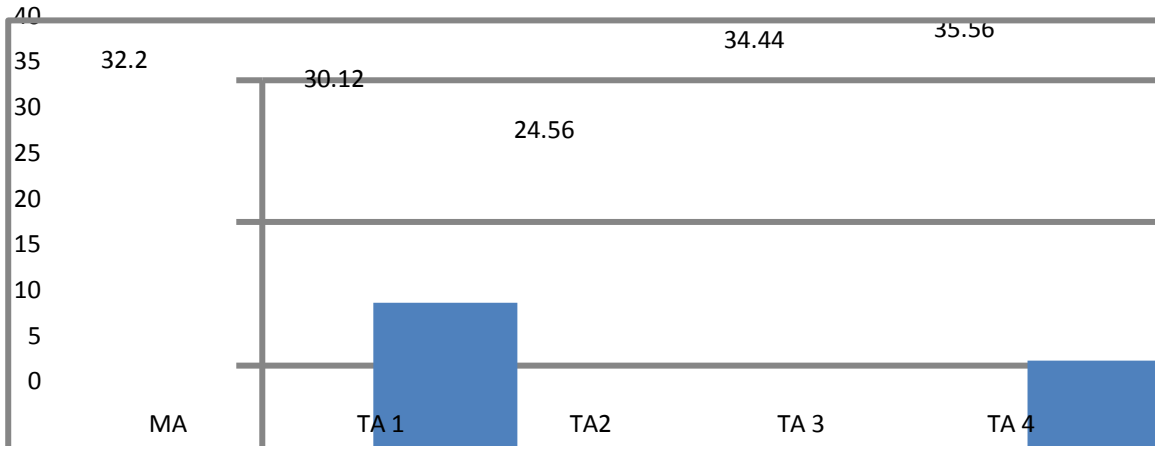

Fig.8 Comparison of PSNR of Lena Image using Different Tolerant adders

Comparison of power consumption and PSNR of different tolerant adder are shown in figure 9.

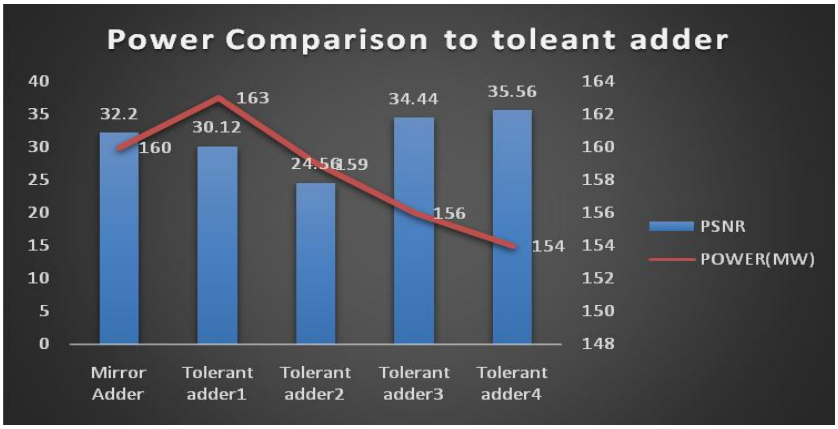

Fig.9 Comparison of PSNR and Power for Different Tolerant Adders

IV. CONCLUSION

In this paper, we proposed several imprecise or tolerant adders that can be effectively utilized to trade off power and quality for error-resilient DSP systems. Our approach aimed to simplify the complexity of a conventional MA cell by reducing the number of transistors and also the load capacitances. When the errors introduced by these approximations were reflected at a high level in a typical DSP algorithm, the impact on output quality was very little. Note that our approach differed from previous approaches where errors were introduced due to VOS [3]–[10]. A decrease in the number of series connected transistors helped in reducing the bits in each case are accurate. According to our experiments, using approximate FA cells beyond effective switched capacitance and achieving voltage scaling. We also derived simplified mathematical models for error and power consumption of an approximate RCA using the approximate FA cells. Using these models, we discussed how to apply these approximations to achieve maximum power savings subject to a given quality constraint. This procedure has been illustrated for two examples, DCT and FIR filter. We believe that the proposed tolerant adders can be used on top of already existing low-power techniques like SDC and ANT to extract multifold benefits with a very minimal loss in output quality.

REFERENCES

[1] A. B. Melvin, “Let’s think analog,” in Proc. IEEE Comput. Soc. Annu.Symp. VLSI, 2005, pp. 2–5

[2] International Technology Roadmap for Semiconductors, latest edition available online at http://public.itrs.net/.

[3] A. B. Melvin and Z. Haiyang, “Error-tolerance and multi-media,” in Proc. 2006 Int. Conf. Intell. Inf. Hiding and Multimedia Signal Process., 2006, pp. 521–524.

[4] M. A. Breuer, S. K. Gupta, and T. M. Mak, “Design and error-tolerance in the presence of massive numbers of defects,” IEEE Des. Test Comput., vol. 24, no. 3, pp. 216–227, May-Jun. 2004.

[5] M. A. Breuer, “Intelligible test techniques to support error-tolerance,” in Proc. Asian Test Symp., Nov. 2004, pp. 386–393.

[6] K. J. Lee, T. Y. Hsieh, and M. A. Breuer, “A novel testing methodology based on error-rate to support error-tolerance,” in Proc. Int. Test Conf., 2005, pp. 1136–1144.

[7] I. S. Chong and A. Ortega, "Hardware testing for error tolerant multimedia compression based on linear transforms," in Proc. Defect and Fault Tolerance in VLSI Syst. Symp., 2005, pp. 523–531.

[8] H. Chung and A. Ortega, "Analysis and testing for error tolerant motion estimation," in Proc. Defect and Fault Tolerance in VLSI Syst. Symp., 2005, pp. 514–522.

[9] H. H. Kuok, "Audio recording apparatus using an imperfect memory circuit," U.S. Patent 5 414 758, May 9, 1995. (2002) The IEEE website. [Online]. Available: http://www.ieee.org/

[10] T. Y. Hsieh, K. J. Lee, and M. A. Breuer, "Reduction of detected acceptable faults for yield improvement via error-tolerance," in Proc. Des., Automation and Test Eur. Conf. Exhib., 2007, pp. 1

[11] D. Shin and S. K. Gupta, "Approximate logic synthesis for error tolerant applications," in Proc. Design, Automat. Test Eur., 2010, pp. 957–960.

[12] B. J. Phillips, D. R. Kelly, and B. W. Ng, "Estimating adders for a low density parity check decoder," Proc. SPIE, vol. 6313, p. 631302, Aug.2006

[13] J. M. Rabaey, Digital Integrated Circuits: A Design Perspective. Upper Saddle River, NJ: Prentice-Hall, 1996/

[14] Lyons, V. Ganti, R. Goldman, V. Melikyan, and H. Mahmoodi,"Full-custom design project for digital VLSI and IC design courses using synopsys generic 90nm CMOS library," in Proc. IEEE Int. Conf. Microelectron. Syst. Edu., Jul. 2009, pp. 45–48.

[15] "K. K. Parhi, VLSI Digital Signal Processing Systems: Design and Implementation. New York: Wiley,