COMPARATIVE ANALYSIS OF CMOS JOHNSON COUNTER LAYOUT

Manish Chauhan[1], Rajesh Mehra[2]

[1] M.E Scholar, [2]Associate Professor, Electronics & Communication Engineering, NITTTR, Chandigarh, (India)

ABSTRACT

Area and power minimization are the prime concerns in recent VLSI design. As chip size is shrinking and many other micro-electronics reliabilities are developing gradually, low power and small area design of any system has become priority. The performance of flip-flop is an important element to determine the efficiency of the whole synchronous circuit. In this paper, an area efficient layout design of Johnson Counter has been proposed. Area of Johnson Counter has been compared using auto generated, semi custom and fully custom layout design techniques. It is analyzed that fully custom layout shows the improvement of 67 % in area consumption than auto generated. It is also clear from the simulation results that the power reduction of 28% in fully custom as compare to semicustom layout design.

Keywords: CMOS, Counter, Flip-Flop, Johnson Counter, Sequential Circuit.

I. INTRODUCTION

All the arithmetic, logical and memory processes are performed in computer system synchronously according to the clock cycle. So, effective design of sequential circuits is very important for the best performance of any computer system. Various kinds of counters and registers are considered as sequential circuits [1]. A digital counter whose states change according to the pulse applied at the input to the counter. A counter is one of the more useful digital circuits. Counters are used in many applications like frequency dividers, and frequency counters and a quick example of a digital counter is stopwatch [2]. Different counter systems are very important as they provide different data sequences synchronously. These kinds of sequences are required in various logic designs. A counter is a registered circuit. This implies that the counter circuit is a finite state machine (FSM). Therefore, it has several discrete states that it can be in [3].

The basic memory element in sequential logic is the flip flop and these flip flops stores the data on both the rising and falling edge of the clock pulse. If the flip flops stores the data on rising or falling edge of clock then it is said to be single edge triggered and if the flip flops stores the data on both rising and falling edge then it is said to be double edge triggered flip flops [4]. In VLSI design low power and area efficient circuit design plays a very vital role in modern days. The proper architecture of sequential circuits using minimum number of CMOS logic gates design low power circuits [5]. Total power consumption is based upon the power consumed by the flip flops. The design technique and the flip flop choice have a great impact on the power reduction [6]. At the beginning of VLSI design power dissipation was not a very important issue. In earlier days performance and area were the more consideration part for the VLSI designer. But as the system area is shrinking gradually and clock frequency is developing rapidly, power issue has become one of the prime concerns for system designers [4].

In VLSI design binary sequence counter is very essential building blocks. The principle on which binary sequence counter based is synchronous timing of clock cycle through which data is evaluated and assigned to its associated flip flop [2]. Setup time and hold time are the two main time constraints to sample the data correctly for the flip flops [7]. By using of conventional flip flops counters suffer the problem of power consumption. Conventional flip flops not only increase the power but also increases the area and design complexity [8].

II. JOHNSON COUNTER

Johnson counter is also known as a twisted ring counter or mobius counter, connects the complement output of last shift register to the input of first register and circulates the streams of one's followed by zeroes around the ring. Counter is a device that stores the number of times a particular event or process has occurred often in relation to a clock signal. In all the digital circuits counters are used in almost for counting operations. There are many types of counters used in digital circuits. Johnson counter or twisted ring counter is the modified form of a ring counter [9]. The main difference between ring counter and Johnson counter is that in ring counter the output of last shift register is fed to the input of the first shift register, but in case of Johnson Counter the complement output of last shift register to the input of first register. In four bit ring counter one of the register must be preloaded with one or zero and the bit pattern is 1000, 0100, 0010, and 0001. An n-bit synchronous Johnson counter is built up by cascading n D flip flops with same clock [5]. The initial value of register is 0000 and the bit pattern of 4-bit Johnson Counter is 1000, 1100, 1110, 1111, 0111, 0011, 0001 and 0000. The 4 bit Johnson Counter is shown in Fig.1.

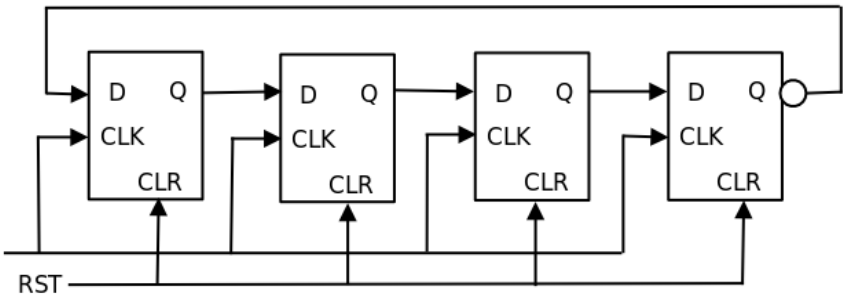

Fig.1 Four bit Johnson Counter

Table 1: Truth table of 4-bit Johnson Counter

State	Q0	Q1	Q2	Q3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0

This paper proposes the design of area efficient 2-bit Johnson Counter using three different techniques. Further if the result is optimal then this 2-bit design can be implemented for higher bits counter. The two bit Johnson counter is shown in Fig.2.

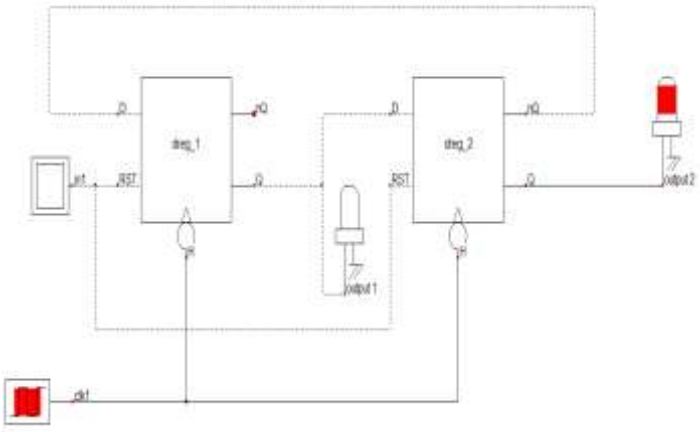

Fig.2 Two Bit Johnson Counter

Three different methods are implemented using DSCH and Microwind software. The DSCH2 program is a logic editor and simulator and used to validate the architecture of the logic circuit before the microelectronic design is started. DSCH2 provides a user friendly environment for hierarchical logic design and simulation with delay analysis, which allows the design validation of complex logic structures. Microwind2 software allows designing and simulating an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate Microwind2 includes all the commands for a mask editor as well as original tools never gathered before in a single module (2D and 3D process view, VERILOG compiler, tutorial on MOS devices). The electric extraction of circuit is automatically performance and the analog simulator produces voltage and current curves immediately [10].

III. LAYOUT DESIGN SIMULATION

The first method of designing the Johnson Counter in DSCH and generating its verilog file. Now in Microwind this verilog file is compiled and auto generated layout is created. In Microwind software different foundries are available in the library. In this paper cmos 90 nm foundry is selected. The auto generated layout of Johnson counter is shown in Fig.3.

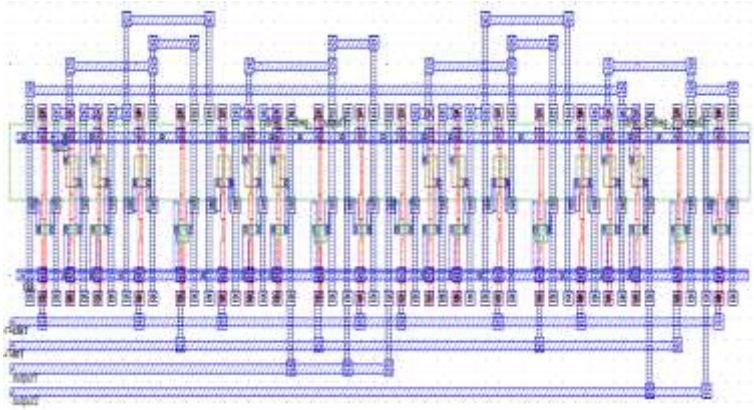

Fig.3 Layout of 2- bit Johnson Counter

This layout is checked for DRC and if there is no error present in the layout then the layout is stimulated. The output of simulation is checked with the output of 2-bit Johnson Counter then further check the power and area of auto generated layout. The measured power here is 96.333 µW and the area consumed here is 269.9 μm^2. The output of Johnson Counter is shown in Fig.4.

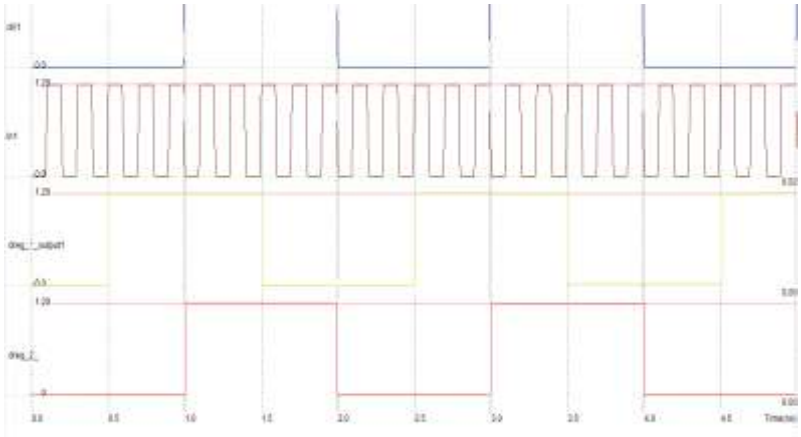

Fig.4 Output of Auto Generated layout

The second step is to directly make use of in built transistors available in the Microwind software. In this method the connections are made by the developer and hence there is a large possibility that area may get reduced. The semi scustom layout using the in- built transistors i.e. N- MOS and PMOS is shown in Fig.5.

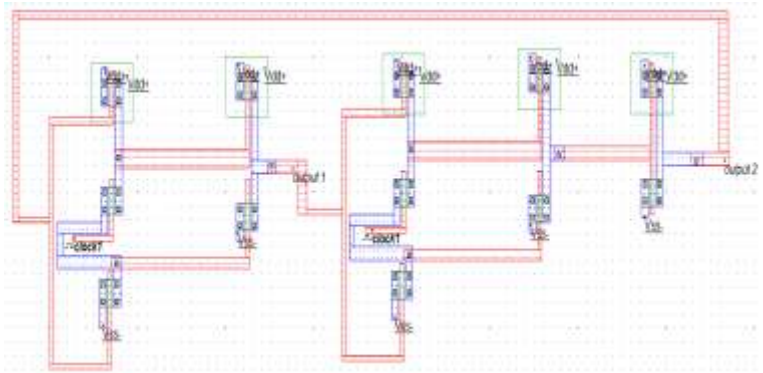

Fig.5 Semi Custom Layout

When the layout is ready it is again checked for DRC and if there is no error present in the layout, the circuit is simulated and the outputs are obtained. The obtained output is verified with the truth table of Johnson Counter. If the truth table is verified we can further check the power and area consumed. The measured power is 0.145 mW and the area consumed is 134.3 μm^2. The output of semi custom layout is shown in Fig.6.

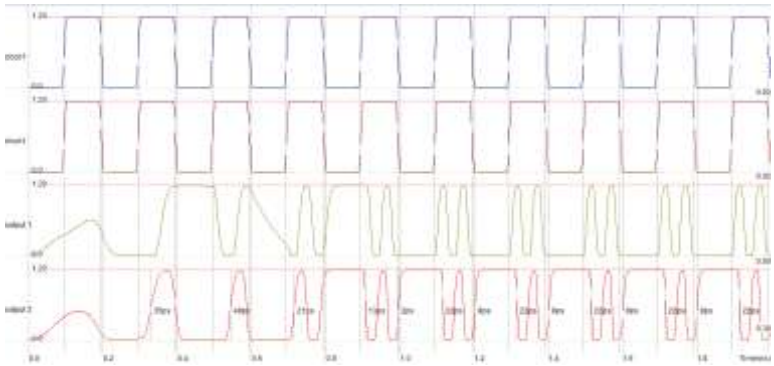

Fig.6 Output of Semi Custom Layout

The third method is to create our own N- MOS and PMOS transistors. Here the created transistors are called from the library and then connections are made. The fully custom layout using the self created transistors i.e. N-MOS and PMOS is shown in Fig.7.

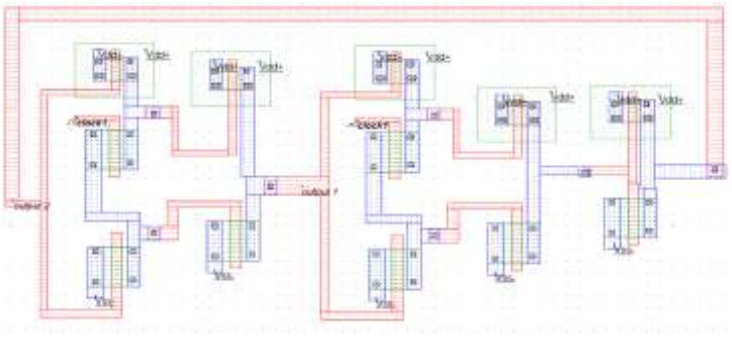

Fig.7 Fully Custom Layout

When the layout is ready it is again checked for DRC and if there is no error present in the layout, the circuit is simulated and the outputs are obtained. The obtained output is verified with the truth table of johnson counter. If the truth table is verified we can further check the power and area consumed. The measured power is 0.104 mW and the area consumed is 90.4 μm^2. The output of fully custom layout is shown in Fig.8.

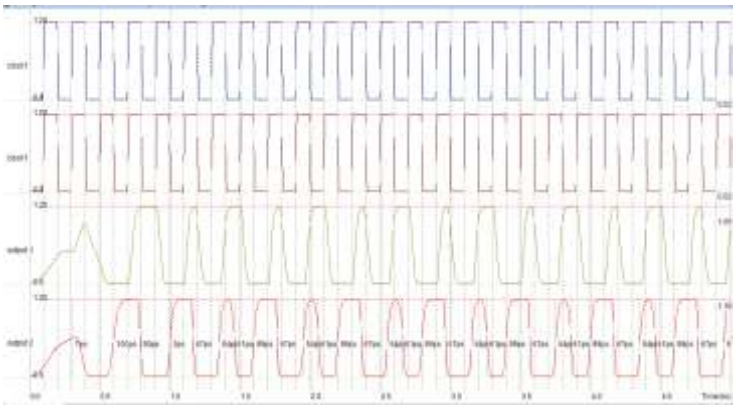

Fig.8 Output of Fully Custom Layout

IV. RESULT ANALYSIS

In this section, the area and power of different layout design has been compared using three different methods based on simulation results. A comparative analysis of table 2 shows that the power of fully custom layout design is more as compare to auto generated. But on the other side there is reduction of 67% in area. Tabular method chart have been used to compare the results.

Table 2: Comparison of Area and Power

PARAMETER	AUTO GENRATED	SEMI CUSTOM	FULLY CUSTOM
POWER	96.333 µW	0.145 mW	0.104 mW
AREA	269.9 μm^2	134.3 μm^2	90.4 μm^2

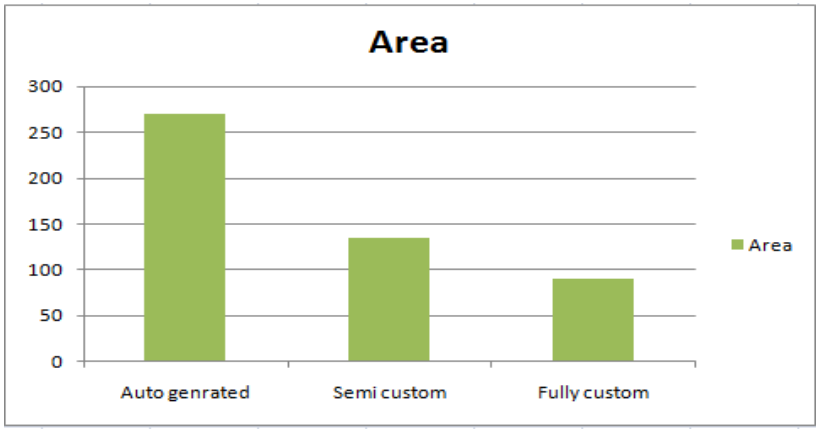

Fig.8 Bar Chart Comparison of Area

V. CONCLUSION

In this paper, the auto generated layout design consume less power as compare to the semicustom layout design but the area consumption is 49.77% more than semi custom layout design technique. When auto generated layout is compared to fully custom layout design than there is a reduction of 67% in the area. The comparative analysis in terms of area the fully custom consumes 32.68% less area than the semi custom layout design technique. It is clear from the simulation results that the fully custom layout design is more efficient in terms of area. So fully custom layout design technique can be implemented in the applications where area reduction is the main consideration. Here power factor can be compensated for area.

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AUTHORS

Manish Chauhan received the B.Tech degree in Electronics and communication from P.T.U, Jalandhar, India in 2010. He is pursuing his M.E in Electronics & Communication from National Institute of Technical Teachers Training & Research, Chandigarh India. His current research interests focus on VLSI Design

Rajesh Mehra received the Bachelors of Technology degree in Electronics and Communication Engineering from National Institute of Technology, Jalandhar, India in 1994, and the Masters of Engineering degree in Electronics and Communication Engineering from National Institute of Technical Teachers' Training & Research, Punjab University, Chandigarh, India in 2008. He is pursuing Doctor of Philosophy degree in Electronics and Communication Engineering from National Institute of Technical Teachers' Training & Research, Punjab University, Chandigarh, India.

He is an Associate Professor with the Department of Electronics & Communication Engineering,, National Institute of Technical Teachers' Training & Research, Ministry of Human Resource Development, Chandigarh, India. His current research and teaching interests are in Signal, and Communications Processing, Very Large Scale Integration Design. He has authored more than 175 research publications including more than 100 in Journals. Mr. Mehra is member of IEEE and ISTE.