CMOS LAYOUT DESIGN OF AREA EFFICIENT SYNCHRONOUS DOWN COUNTER

Ritesh Pawar[1], Rajesh Mehra[2]

[1] M.E Scholar, [2] Associate Professor, Electronics & Communication Engineering, NITTTR, Chandigarh, (India)

ABSTRACT

Counter is a fundamental function of digital circuits. A digital counter consists of a collection of flip-flops that change state in a prescribed sequence. The counter is provided with additional synchronous clear and count enable inputs. This paper presents the design of 2 bit synchronous down counter with low area and power requirement. D flip-flop is used for designing of 2 bit synchronous down counter and the results of self developed layout are compared with the results of auto generated layout in 90nm technology. The self developed counter layout has shown the improvement in area of 15.07%

Keywords: Down Counter, D- Flip-Flop, XOR, Synchronous, CMOS

I. INTRODUCTION

Now a day's electronics engineers put their more focus on the performance and area of the circuits. On the hand more importance given to the reliability and cost of the design, but power consumption is a peripheral consideration for the designers. In the present days or years this is to be changed more rapidly and equal importance given to the power as compared to the area and speed [1]. For VLSI designing static CMOS circuits designed in the logic gates of the integrated circuits with the help of the nMos, pMos pull-up pull-down networks. Due to the tendency of the good noise margins and are fast, low power, easy to design are widely give their support for the designing [2].For counting the pulses the digital circuit which is used is known as the Counter. In the flip-flops the most common application is Counter. In a digital circuit it is one of the most useful circuits. They are widely used in the many applications. The most common examples are frequency dividers and frequency counters. The following characteristics of the digital counters may be defined but most common characteristics is that it counts maximum numbers before it rolls over (returns to zero). It is also known as counter's modulus. The digital counter counts in either direction i.e. (ascending from low to high or high to low). It can be either in the asynchronous or synchronous. This means that it counts with the help of the system clock, or independently to the system clock. It can function either as a monostable or an astable circuit. It also behaves like as it runs once and stops or it will run forever until interrupted [3].

Instead of the use of low supply voltages, the continuous increase of clock frequency can cause more power consumption. Due to leakage of inactive devices static component forms power consumption and from switching of active devices dynamic components formed. The design of Counters is generally formed with the help of the flip-flop [4]. Now they are divided in two categories like in synchronous and asynchronous also further depends on the flip-flops clock application. Synchronous counter is used in this paper. The clock input for all stages of flip-flop in synchronous down counter is given by a single clock. At the same time all stages

outputs are changed. The process of obtaining the output in asynchronous counter is as that it takes the input as a clock for the next stage with the help of the previous stage; therefore in asynchronous counters for all stages the output ripples to forms the final output [5].

Battery powered devices are used in the latest advanced technology of the mobile, like personal digital assistant (PDA) mobile and another portable electronic devices. In VLSI circuit designing power-delay played an important role for the mobile devices because they required high speed and low power consumption. The output power reduction is the optimal method for the operation of low frequency circuits in the sub-threshold region, Due to this in transistor majority carriers repelled from gate area and forms the minority carrier channel in the transistor. Therefore this process is known as the strong-inversion, by the formation of the more minority carriers as compared to the majority carriers. When V_{TH} is more than V_{GS} there is less minority channel, by the presence of these channels they comprises a current and the state which is formed is known as weak-inversion. But in the designing of the standard CMOS design, the current produced in this state is a sub-threshold parasitic leakage, but in case of the voltages the drain voltage V_{DD} lowered below the threshold voltage V_{TH}, So the designed circuit use which can be operated by using the sub-threshold current with ultra-low power consumption [6].

II. COUNTER DESIGN

A set of unique output combinations which are produced by a counter circuit that corresponds to the Many applied input pulses. When counter counts the number of unique outputs then they are known as counters mod or modulus for the designing of the synchronous counter mostly D flip-flops or toggle flip-flop are used. These designed flip-flops generally known as “Synchronous Counters” due to the reason that same clock inputs cannot given to its input clock. When asynchronous counters appears the data in “ripple” form that is the output of one flip-flop given as input of next then they are called as ripple counters[7].

The outputs of synchronous counter changes simultaneously when operation are provided by all flip-flops and so instructed by the steering logic. These operations caused the eliminations of the output counting spikes which are associated with the help of the synchronous counter or “ripple clock” counter [8]. When enable input is low the output of the flip-flop triggered on a low to high level transition of the clock input. In the counter clock is high, when enable input starts counting. The counter counts up when input is low, and its counts down when it is high [9]. The synchronous counter is fully programmable; which means that counters preferably be preset by the help of placing the low level load input and it enters the use full data into data inputs.. The level of the clocked input changes independently by the help of previous stage output. Due to this reason the synchronous counters can be used as modulo-N dividers with changed in the count length by the help of preset inputs. When the clock goes up/down, the load input buffered to lowers the input requirement; and also reduces the number of clock drivers which are required for the long length parallel words [10],[11].

In the down counter the next state is driven from the previous state. Here in the above table the example is taken as that if the previous state is 1 1 then in down counter the next state is 1 0. Similarly if the next stage is previous state i. e 1 0 then its next state is 0 1.

Table 1. Truth Table of Down Counter.

Present State		Next State		Inputs	
q0	**q1**	**Q0**	**Q1**	**D0**	**D1**
1	1	1	0	1	0
1	0	0	1	0	1
0	1	0	0	0	0
0	0	X	X	X	X

The figure 1 shows the schematic design of 2 bit down counter. In this design two flip-flops are used. These two flip-flops are of D type. In this design one XNOR gate is also used for the input of the first d flip-flop. These two d flip flop has common clock input. Here d flip-flop is described as D_A and D_B. The D_A and D_B flip flop has common switch which behaves as a reset in the circuit to clear the previous value.

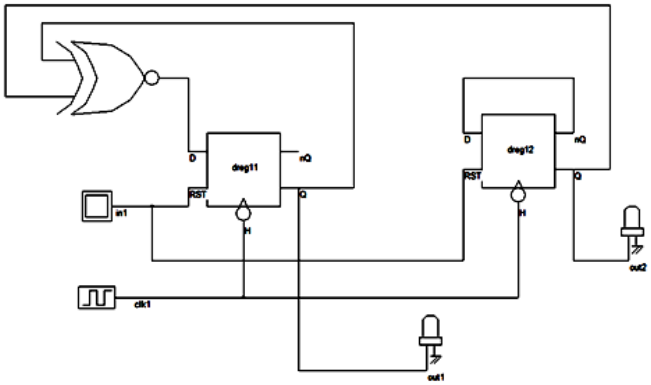

Figure 1. Schematic Design of Down Counter

In this paper a 2 bit down counter has been implemented using two different ways. This paper proposes the design of area efficient of 2 bit down counter. Further if the results are optimal then this two bit down counter design can be implemented for the lower bits of the down counter. The two different methods are implemented in the software. The first is used to validate the architecture of the logic circuit before the microelectronics design is started. It provides a user friendly environment for hierarchical logic design, and simulation with delay analysis, which allows the design and validation of complex logic structures. The second method provides a program that allows designing and simulation and integrated the circuit at physical description level. The Package contains a library of common logic and analog ICs to view and simulate. The second method includes all the commands for mask editor and for verilog compiler. So can be access to circuit simulation by pressing one single key. The electric extraction of the circuit is automatically performance and the analog circuits.

III. LAYOUT DESIGN SIMULATION

The first method is the designing of the down counter n software and then generating its verilog file. Now in second method this verilog file is compiled and an auto generated layout is created. By nm. The layout design of

generated counter is shown selecting the different foundries which are available in the library of the software. Here the foundry is selected is 180 below.

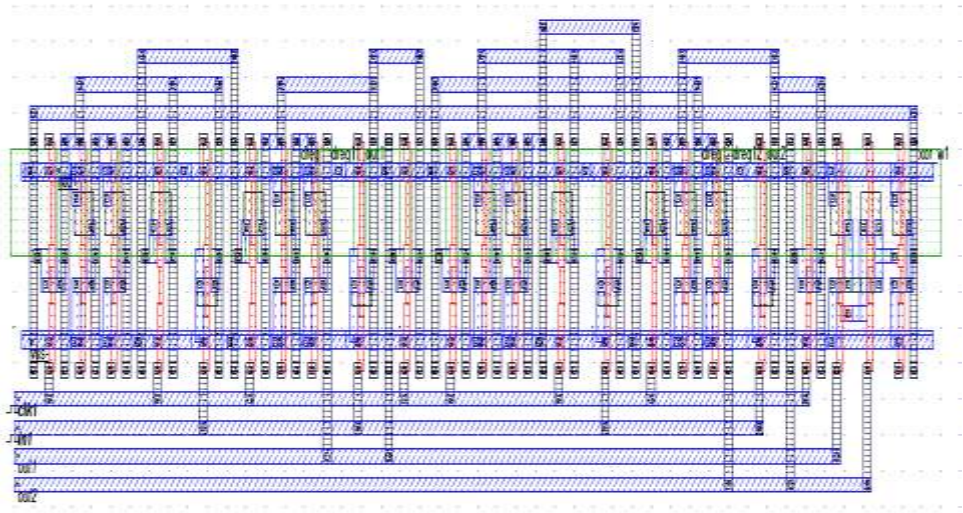

Figure 2. Auto Generated 2- Bit Down Counter

This layout is checked for the DRC and if there is no error present in the layout it is simulated. The output of the simulation is checked and if the output matches the output of the 2 bit down counter then further check the power and the area of this auto generated layout of 2 bit down counter.

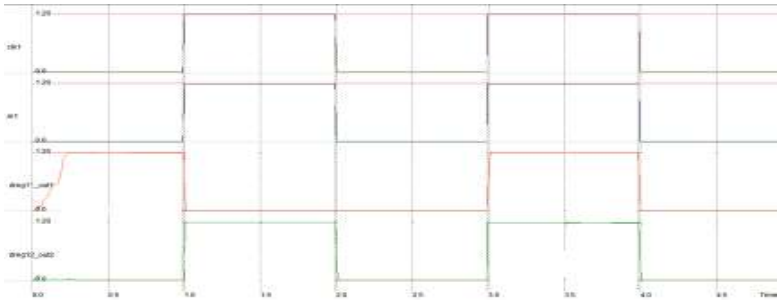

Figure 3. Output of Auto Generated 2- Bit Down Counter.

The figure 3 shows the output of the 2 bit down counter. Also power can be measured from the result of simulation. The measured power here is 84.194µw. The area consumed here is 159.1µm^2. Now the second step is to directly make use of inbuilt transistor available in the Microwind software. In this method the connections are made by the developer and hence there is a large possibility that area may get reduced.

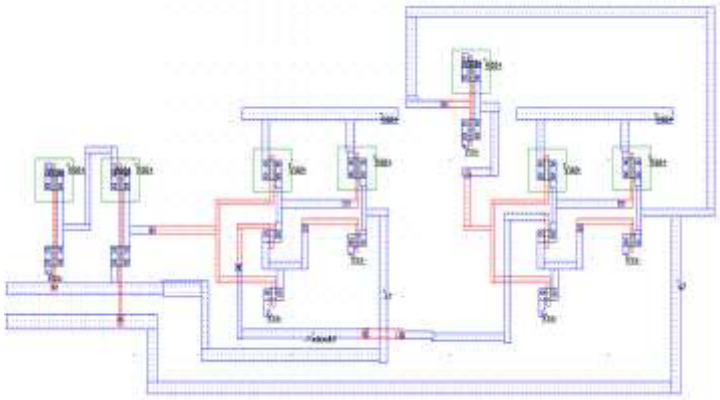

Figure4. Self Generated 2 Bit Down Counter

When the layout is ready it is again checked for DRC and if there is no error present in the layout, the circuit is simulated and the outputs are obtained. The obtained output is verified with the truth table of 2 bit down counter. If the truth table is verified and further check power and area.

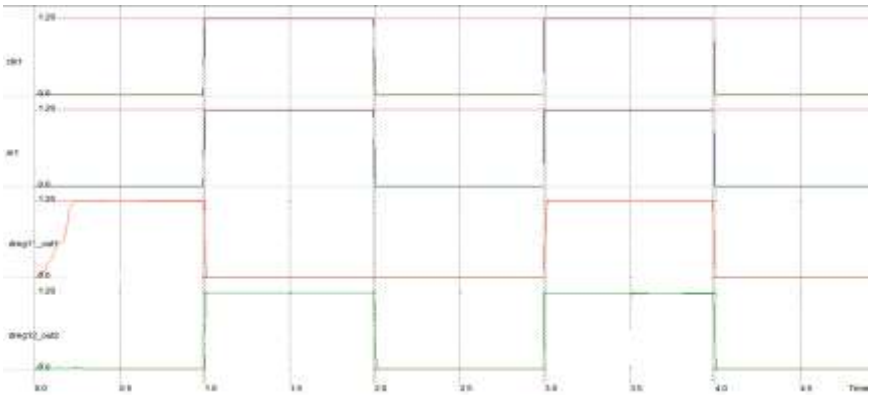

Figure 5. Output of Self Generated 2- Bit Down Counter.

Now check the result for power and area. Here the power consumed is 0.699µw. The area consumed by this layout is 135.12µm^2. As shown in figure 4, 5.

IV. RESULT AND DISCUSSION

A comparative study can be done on analysis the above results for power and area obtained by using these methods. The basic comparison is done in between the self generated and auto generated layout of the 2 bit down counter.

Table 2. Comparative Analysis of Area And Power Consumption In 2 Bit Down Counter.

Parameter	Auto generated Layout	Semi Custom Layout
Power	84.194µw	159.1µm^2
Area	0.699mw	135.12µm^2

A comparative analysis of this table shows that in terms of area , the layout genrated using in- built transistors is increasing. But on the other hand in terms of the power genrated layout is using less power in comparison to the layout using in –built transistors and self created transistors. There is a reduction of 15.07% in area when auto genrated layout is compared to the layout of the in built transistors. When auto genrated layout is compared to layput using self created transistors then there is one drawback occurs is that it incresed the power of the layout design by the factor of the 7.3%.

V. CONCLUSION

In this paper the D flip-flop is designed with the help of large number of PMOS and NMOS transistors. This has been used to design area efficient synchronous down counter for the various applications. For this designing

purpose CMOS 90nm fabrication technology has been used which is compared with the auto generated design for the same circuit. It has been found that the purposed design consume 135.12µm^2 area while the auto generated counterpart consuming 159.1µm^2 area on silicon. However the design circuit a bit more power as compared with the auto generated design. In the case of power the drawback of the self generated layout is increased by the factor of 7.3%.

VI. ACKNOWLEDGMENT

The author would also like to thank Director, National institute of Technical Teachers' Training & Research Chandigarh, India for their inspirations and support on this research work

REFERENCES

[1] Paanshul Dbriyal, Karan Sharma, Manan Sethi, Geetanjali, " A high performance D flip-flop design with low power clocking system using MTCMOS technique", 3rd IEEE International Advance Computing Conference(IACC), Vol. 1, pp. 1524-1528, 2013.

[2] Niel H. E. Weste, David Harris, Ayan Benerjee, "CMOS VLSI Design ", Pearson Education, New Delhi, pp. 342-337, 2009.

[3] Upwinder Kaur, Rajesh Mehra, "Low power CMOS counter using clock gated flip-flop", International Journal of Engineering and Advanced Technology, Vol.2, pp. 796-798, April 2013.

[4] K.G.Sharma, Tripti Sharma, B.P.Singh, Manisha Sharma, "Modified SET D-Flip Flop Design for Low-Power VLSI Applications", Indian International conference on Power electronics, IEEE, pp 1-5, 2011.

[5] Sung-Mo Kang , Yusuf Leblebici, "CMOS Digital Integrated Circuits ", Tata McGraw-Hill publication New Delhi, pp. 343-347, 2010.

[6] Narendra S., Tschanz J., Hofsheier J., Bloechel B., Vangal, S., Hoskote Y., Tang S., Somasekhar D., Keshavarzi A., Erraguntla V., Dermer G., Borkar N., Borkar S., De V., "Ultra-low voltage circuits and processor in 180nm to 90nm technologies with a swapped-body biasing technique", Solid-State Circuits Conference, IEEE International, Vol.1, pp. 156-518, 15-19 Feb 2004.

[7] Ranjeeta verma, Rajesh Mehra, "CMOS based design simulation of adder/subtractor using different foundries," International journal of science and engineering IEEE Trans. on VLSI Systems, Vol. 2, pp. 28-34, Nov.1 2013.

[8] Yogita Hiremath, Akalpita L. Kulkarni, J. S. Baligar," Design and Implementation of Synchronous 4 bit up Counter using 180NM CMOS Technology",International Journal of Research in Engineering and Technology, Vol. 3, pp. 810-815, 5 may 2014.

[9] Manoj Sharma, Dr Arti Noor, Shatish Chandra Tiwari, and Kunwar Singh, "An Area and Power Efficient design of Single Edge Triggered D-Flip Flop", in Proc. IEEE International Conference on Advances in Recent Technologies in Communication and Computing, pp. 478 – 481, 2009.

[10] Priyanka Sharma, Rajesh Mehra,"True single phase clocking based flip-flop design using different foundries", International Journal of Advance in Engineering & Technology, Vol. 7, pp. 352-358, May– 2014.

[11] Praween Sinha, Shreyaansh Srivastava, "Design of a Low Power Four-Bit Binary Counter Using Enhancement Type Mosfet", International Journal of Engineering Research & Technology, Vol.1, pp. 1-6, October 2012.

AUTHORS

Ritesh Pawar received the B.Tech degree in Electronics and communication from P.T.U, Jalandhar, India in 2010. He is pursuing his M.E in Electronics & Communication from National Institute of Technical Teachers' Training & Research Chandigarh India. His current research interests focus on Digital Signal Processing.

Rajesh Mehra received the Bachelors of Technology degree in Electronics and Communication Engineering from National Institute of Technology, Jalandhar, India in 1994, and the Masters of Engineering degree in Electronics and Communication Engineering from National Institute of Technical Teachers' Training & Research, Punjab University, Chandigarh, India in 2008. He is pursuing Doctor of Philosophy degree in Electronics and Communication Engineering from National Institute of Technical Teachers' Training & Research, Punjab University, Chandigarh, India.

He is an Associate Professor with the Department of Electronics & Communication Engineering,, National Institute of Technical Teachers' Training & Research, Ministry of Human Resource Development, Chandigarh, India. His current research and teaching interests are in Signal, and Communications Processing, Very Large Scale Integration Design. He has authored more than 175 research publications including more than 100 in Journals. Mr. Mehra is member of IEEE and ISTE.