FPGA BASED DESIGN OF MEDIAN FILTER TO REDUCE NOISE IN IMAGING

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ABSTRACT

In this paper it is necessary to perform high degree of noise reduction in an image as well as preserving the edges from corrupted image as presented here. In the signal transmission the image signal can be corrupted by noise and the blurred image occurs. The Median filter is a nonlinear digital filtering technique often used to reduce speckle noise and salt and pepper noise from images without damaging the edges. The simulation design gives better image and it is simple to implement.

Key Words: FPGA, Impulsive noise, Logic devices, Median filter, VHDL

I. INTRODUCTION

Digital image processing refers to processing digital images on digital computer. As a subfield of digital signal processing, digital image processing has many advantages over analog image processing; it allows a much wider range of algorithms to be applied to the input data, and can avoid problems such as the build-up of noise and signal distortion during processing. Most images involve two dimensional functions and applying standard signal-processing techniques to it. Image Processing is a signal processing in which inputs and outputs are images such as photographs or frames of video. Also some methods whose inputs may be images but output are extracted from those images. There are various methodologies that can applied to images for different purposes such as image acquisition, image enhancement, image restoration, etc. Images are always preferred to texts in multimedia transmission but all these communications face a common problem: "Noise". One of the most common forms of noise is the impulse noise, also known as salt and pepper noise which is caused because of noisy pixel value is either minimum or maximum value. There have been many methods for removing salt-and-pepper noise, and some of them perform very well. Our main goal is to remove the fixed-valued impulse noise from the corrupted images. Recently, many image de-noising methods have been proposed for impulse noise suppression.The median filter was once the most popular nonlinear filter for removing impulse noise, because of its good denoising power and computational efficiency. However, when the noise level is over 50%, some details and edges of the original image are smeared by the filter. Filters are chosen according to their noise pattern in the field of image processing. Hardware implementation can result better speed with the help of pipelining and parallelism technique than the software implementation. Reconfigurable nature of FPGAs consisting with pipeline and parallelism technique makes it efficient to reduce the complexity of algorithms and

simplify the debugging and verification. In this paper, the algorithms of median are proposed in the means of hardware implementation for removal of impulse noise considering salt and pepper noise from images.

II.MEDIAN FILTER

Median Filter is a spatial filtering operation, so it uses a 2-D mask that is applied to each pixel in the input image Its strength lies in its ability to filter out impulsive noise without destroying the properties of the underlying signal. It is used to remove defects and noise from pictures. Median filter is much less sensitive than the mean to extreme values (called outliers), therefore it is better without reducing the sharpness of the image and edge preserving nature. Edge detection typically is followed by linking algorithms designed to assemble edge pixels into meaningful edges or region boundaries. The FPGA and PLD's are rising applications in all fields of engineering because of their high speed parallel operations. This paper presents a fast and efficient processing architecture based on FPGA for the filtration of the impulsive noise. In noise filtering, the essential plan is a manner to preserve some desired signal selections whereas attenuating the noise. A block diagram of median filter is depicted in Figure 2.1.

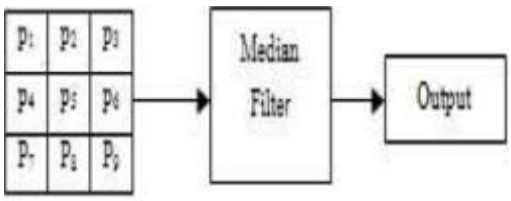

Figure 2.1 Block Diagram of Median Filter

Traditionally, the impulse noise is removed by a median filter which is the most popular nonlinear filter. To apply the mask means to center it in a pixel, evaluating the covered pixel brightness and determining which brightness value is the median value. The algorithm is: every pixel from the picture to be filtered is replaced by the median value of the neighbouring pixels. The picture is thus transformed by the median filter by another picture that has exactly the same size. For every pixel P of the input picture we first create a list of the 9 (3x3) pixels surrounding P. The 9 pixels are then sorted. The median value is the value located at the center of the sorted list. The pixel P in the filtered picture takes this median value. In our example the pictures are grayscale pictures, 8 bits per pixel. The pixel values are between 0 (black) and 255(white).

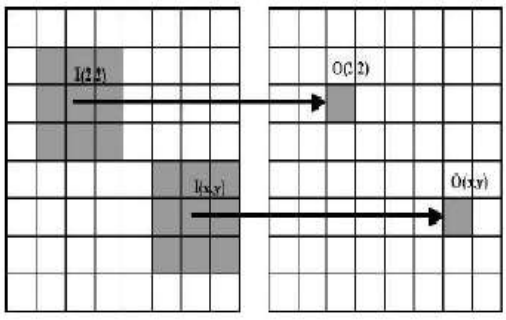

Figure 2.2 The Concept of Spatial Filtering Based on A 3x3 Mask, where i is The Input Image and O is The Output Image.

The median value is determined by placing the brightness in ascending order and selecting the centre value. The obtained median value will be the value for that pixel in the output image. The oldest sample is discarded, a new sample acquired, and the calculation repeats.

III. IMPULSIVE NOISE

Noise is any undesirable signal. Noise is everywhere and thus we have to learn to live with it. Noise gets introduced into the data via any electrical system used for storage, transmission, and/or processing. In addition, nature will always plays a "noisy" trick or two with the data under observation. When encountering an image corrupted with noise you will want to improve its appearance for a specific application. The techniques applied are application-oriented. Also, the different procedures are related to the types of noise introduced to the image.

Impulse noise is caused by malfunctioning pixels in camera sensors, faulty memory locations in hardware, or transmission in a noisy channel. Two common types of impulse noise are the salt-and-pepper noise and the random-valued noise. For images corrupted by salt-and-pepper noise (respectively random-valued noise), the noisy pixels can take only the maximum and the minimum values (respectively any random value) in the dynamic range. There are many works on the restoration of images corrupted by impulse noise. The impulse noise produces fixed values in the pixels which are 0 (pepper noise) and 255 (salt noise). The aim of noise detection module is to detect the noise pixel with the help of threshold value. Each central pixel should be compared with predefined threshold values (Tl & T2) shown in Figure 3 .

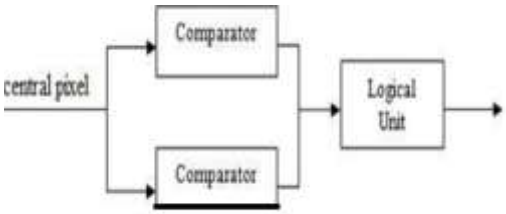

Figure 3.1 Noise Detection Module

The central pixel is considered to be noise free when its value between Tl & T2, Otherwise it is considered as noisy pixel. Another block diagram of impulse noise removal by using FPGA embedded development kit Spartan 3 as shown in figure 3.2

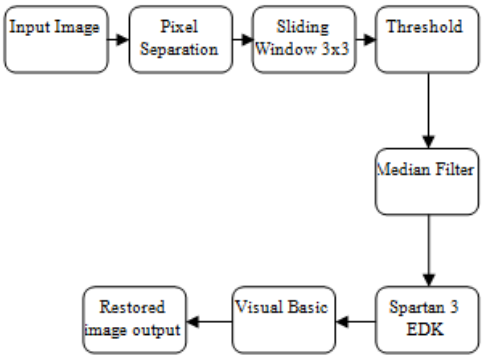

Figure 3.2 Block Diagram of Impulse Noise Removal

IV. HARDWARE IMPLEMENTATION

The VHDL coding of Median Filter and its FPGA implementation is done by Xilinx Synthesis Tool. The Xilinx Platform Studio (XPS) is that the event setting or interface used for developing with the hardware portion of

your Altera DE2 board system. DE2 board is part of the DE2 package in the Altera DE2 Development and education board. The DE2 board has many features that allow the user to implement a wide range of designed circuits, from simple circuits to various multimedia projects. The following hardware is provided on the DE2 board:

• Altera Cyclone II 2C35 FPGA device

• Altera Serial Configuration device - EPCS16

• USB Blaster (on board) for programming and user API control; both JTAG and Active Serial etc.

In addition to these hardware features, the DE2 board has software support for standard I/O interfaces and a control panel facility for accessing various components. In order to use the DE2 board in this project, the user has to be familiar with the Xilinx software. To provide maximum flexibility for the user, all connections are made through the Cyclone II FPGA device. FPGA behaves like processor enforced there on throughout a Xilinx Field Programmable Gate Array (FPGA) device. Thus, the user can configure the FPGA to implement any system design.

V. SIMULATION RESULTS

The VHDL coding of median filtering and its FPGA implementation is done by Xilinx Synthesis Tool. Simulation result for median filter is shown below.

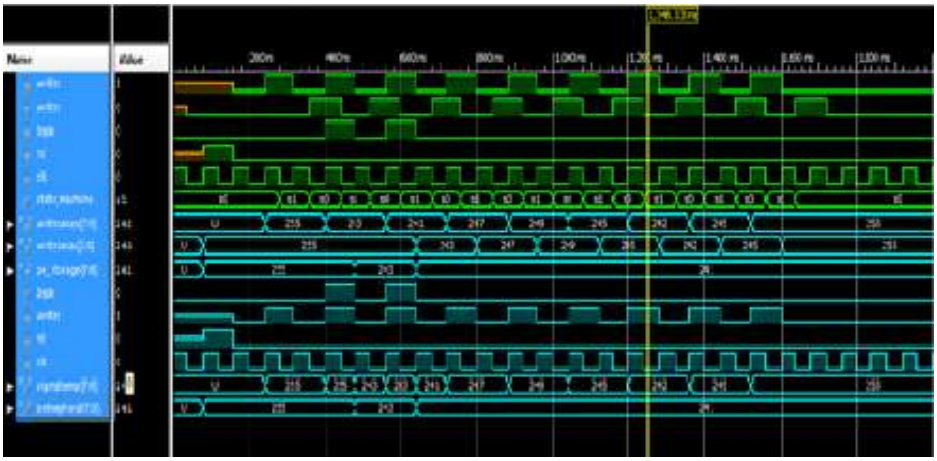

Figure 4.1: Simulation result for Data unit of Median Filter

VI. CONCLUSION

We have presented a novel method for median filtering using FPGA. When the median filter is carried out in real time, the software implementation in general-purpose processors does not usually give good results due to their high computational cost (for sorting N pixels, the temporal complexity is O(N·log N), so the FPGAs are a good alternative (**F**ield **P**rogrammable **G**ate **A**rray -hardware) for median filtering.This paper gives a good description of median filtering FPGA implementation of median filter using VHDL and the sort hardware accelerator made the computation easy, fast and efficient.

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