HIGH SPEED CMOS COMPARATOR

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ABSTRACT

The design & analysis of a latching comparator using dynamic topology for high speed CMOS comparator. The designed dynamic latch comparator is requiring for high speed analog-to-digital converter to get faster signal conversion. This thesis discusses the design and analysis of a high speed dynamic latched CMOS comparator, based on an analytical approach which gives a deeper insight into the associated trade-offs. Simulation results have been obtained by using 90nm technology, considering supply voltage is 1v. The design is simulated by using SPICE tool. Propagation delay is achieved 0.015ns. Power dissipation is 1.1µw, offset voltage is 1.13mv, gain is 55dB achieved.

Keywords: Dynamic Latch, High Speed, Propagation Delay, Comparator

I. INTRODUCTION

This paper present the basic topologies, design decision and the theory needed to understand the latched comparator. The comparator is a critical part of almost all kind of analog-to-digital (ADC) converters. Depending on the type and architecture of the comparator, the comparator can have significant impact on the performance of application. The speed and resolution of an ADC is directly affected by the comparator input offset voltage, the delay and input signal range. Depending on the nature, functionality and inputs, comparators are classified into different four types (1) voltage and current comparators (2) continuous and (3) discrete time comparators etc. Some basic applications of comparators are analog-to-digital conversion, function generation, signal detection and neural networks etc. Comparator is widely used in the process of converting analog signal to digital signals. Low power & high speed ADCs are main building block in front-end of radio-frequency receiver in most of the modern telecommunication system. In the A/D conversion process, it is necessary to first sample the input & then comparator compares the voltages that appears at their input & output a voltage represents the sign of the net difference between them[2].

II. BASIC CMOS COMPARATOR

The schematic symbol and basic operation of a voltage comparator are shown in fig.1. The comparator can be thought of as a decision making circuit. The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison. If the +, VP, the input of the comparator is at a greater potential than the -, VN, input, the output of the comparator is a logic 1, where as if the + input is at a potential less than the – input, the output of the comparator is at logic 0.

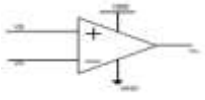

Fig.1: Comparator Operation

This sampled signal is then applied to a combination of comparators to determine the digital to analog signal. Simply we can say that, the comparator can be considered as a 1-bit analog-digital converter. [11],[12].The open-loop comparators are basically op amps without compensation. Regenerative comparators use positive feedback, similar to sense amplifiers or flip-flops, to accomplish the comparison of the magnitude between two signals. A third type of comparator emerges that is a combination of the open-loop and regenerative comparators. This combination results in comparators that are extremely fast. [3],[4].

2.1 Dynamic Latch

Latched means, it uses positive feedback mechanism with one pair of back-to-back cross coupled inverters in order to convert a small input voltage difference to a full scale digital level in less time period. Latched comparator use positive feedback mechanism to regenerates the analog input signal into a full scale digital level output signal.[2]. A dynamic latch is defined as the memory unit that stores the charge on the gate capacitance of the inverter.[1]

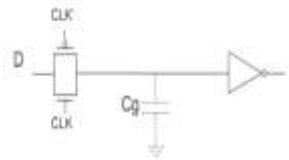

Fig.2 Simple Dynamic Latch

III. LITERATURE REVIEW

Dhanisha N. Kapadia et. al.[13]presented, design of a CMOS charge sharing dynamic latch comparator along with the Buffer stage in 130nm and 90nm technologies. The propagation delay is the time required to the change in output with respect to the change in input. Supply voltage is 1.3v an 0.9v, Propagation delay achieved is 2.13ns & 0.75ns for 130nm & 90nm technology respectively.

Smriti Shubhanand, A.G.Rao et. al.[4]presented, a CMOS comparator that reduces the overall propagation delay & provides higher speed. Here conclude that by using latched comparator design we can increase speed & decrease the propagation delay. Also referring input design circuit, can reduce latch offset voltage & power consumption & hysteresis response. Here, supply voltage is 1v.Propogation delay achieved is 1.787ns.Here 0.25µM technology is used.

Bao-ni Han, Yin-tang Yang, Zhang-ming Zhu et. al.[6]presented, Based on pre-amplifier latch theory, composed pre-amplifier includes positive & negative resistance connected in parallel as its load, a regenerative latch & simple output stage. Multistage open loop comparator is difficult to reach a speed of GSPS (giga sample per second) due to limited bandwidth amplifier. Power supply is 1.8v, maximum offset voltage is 0.6mv and high clock frequency is 1.25GHZ. Here 0.18µM technology is used.

IV. DESIGN PROCESS OF THIS WORK

A high speed latched comparator using positive feedback based back to back latch stage, suitable for pipelined Analog to Digital converter, with reduced delay and high speed is proposed.

During the RESET PHASE, when *Clk* is LOW (*Clk* =0), transistor NMOS_3 is in off state and pmos transistors PMOS_3, PMOS_9, PMOS_4, PMOS_10 are in on state. Transistors NMOS_1 and NMOS_2 are in cut-off mode. Switch transistors PMOS_3, PMOS_9, PMOS_4, and PMOS_10 will charge the drains of transistors

NMOS_ 1 and NMOS_2 and the output nodes Outp and Outn towards *DD V* . During the REGENERATION PHASE, when *Clk* is HIGH (*Clk* =1),

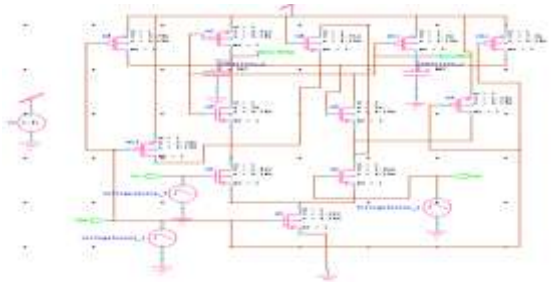

Fig. 3. : High Speed CMOS Comparator

The process starts by turning the transistor NMOS_3 on and immediately an current 'I' starts to flow and the drain of transistor NMOS_3 starts to discharge towards Gnd. In succession the differential input transistors NMOS_1 and NMOS_2 are turned on. The currents of transistors NMOS_1 and NMOS_2 , will start to pull the output nodes Outp and Outn towards Gnd. Due to the difference of voltages between the input signals, the current at the drain terminals of transistors NMOS_ 1 and NMOS_2 will be different. Now in the regeneration mode the output node are discharging Gnd and pmos transistors PMOS_1 and PMOS_2 will come in saturation mode as the voltage at output nodes falls below | | *DD tp V – V* . So a strong positive feedback will enhance the output signal. This regeneration process is completed when one Nmos transistor comes in cut off mode. The design is simulated using 90nm CMOS Technology using Tanner EDA Tools. Proposed design exhibits reduced delay and high speed with a 1.0 V supply. This design can be used where high speed and low propagation delay are the main parameters.

IV. SIMULATION RESULTS

The design is simulated in the design is simulated in 0.25µm CMOS Technology using Tanner EDA Tools. Comparator design shows reduced delay and high speed with a 1.0 V supply. Finally simulation results of the comparator are given below, when a differential signal is applied as an input to the latched comparator. The simulated results are shown below

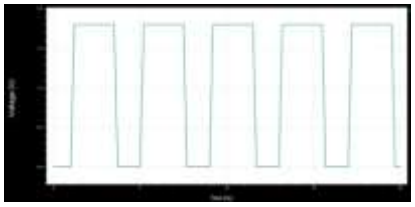

Fig.4 clk

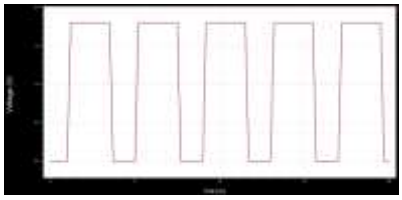

Fig. 5 vin

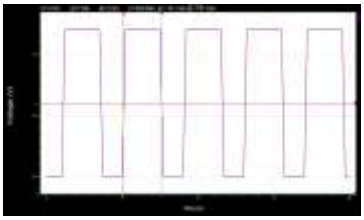

Fig 6 output waveform TLH

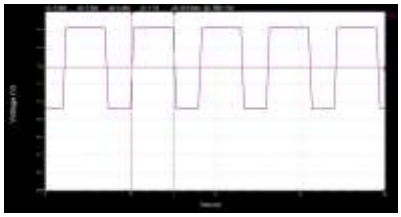

Fig 7 output waveform THL

For, this simulation result, Where TPHL and TPLH are the time difference between 50% of the output and 50% of the input.

tlh = 5.09-5.07 = .02ns, thl = 7.59-7.58 = .01ns

Total propagation delay=0.02+0.01=0.03/2=0.015ns.For this simulation propagation delay is 0.015ns.

V. PERFORMANCE COMPARISON

SPECIFICATION	Present work	Present work	Previous work[1]
Technology	0.18 µm	90nm	90nm
Topology	Dynamic latch	Dynamic latch	Charge Sharing Dynamic Latch Comparator
Input voltage	1.8v	1v	0.9v
Power dissipation	6.6mv	1.1µw	4.89mw
Gain	64db	55db	-
Offset voltage	-	1.13mv	-
Propagation delay	0.56ns	0.015ns	0.75ns

This table gives the comparison between 90nm &0.18µm CMOS technology for respective parameter.

VI. CONCLUSION

This paper presents High Speed Dynamic Latch Comparator fundamentals along with scope of improvement.. One of its features is that, it's using less no. of transistor and improve W/L ratio of transistor. Hence, speed of comparator is increases.

Following Limitations of this are observed:

1. Decrease no. of transistor
2. Improve W/L ratio of transistor

The core focus of this paper is to provide solution to above mentioned limitations for high speed comparator. So to achieve above limitation, different W/L ratio is used according mathematical equation. By using mathematical operation achieved different value of W/L, by simulating that result propagation delay will decrease.

VII. ACKNOWLEDGEMENT

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