AREA EFFICIENT CMOS DESIGN ANALYSIS OF SYNCHRONOUS UP COUNTER

Pragati Gupta[1], Rajesh Mehra[2]

[1]M.E Scholar, [2]Associate Professor, Department of Electronics & Communication Engineering, NITTTR, Chandigarh, UT, (India)

ABSTRACT

This paper presents the design of synchronous up counter which is one of the essential building block in very large scale integration design.Due to increase in demand of portable devices the research of less complex design also increased.Inthis paper Schematic and layout of 2 bit synchronous up counter has been designed using two schemes, one in which D flip flop is made by NMOS and other in which D flip flop is made by transmission gate.Performance of the 2 bit synchronous counter is also analysed in this paper by comparing the auto generated layout and proposed layout using 90nm CMOS technology.The proposed design of synchronous counter is 52.16% more area efficient than the auto generated layout.

Keywords: CMOS Integrated Circuit, Flip-Flops, Intergrationvlsi, Layout and Semiconductor Counter

I. INTRODUCTION

Very-large-scale integration (VLSI) is the process of creating an integrated circuit (IC) by combining thousands of transistors into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. Before the introduction of VLSI technology, most ICs had a limited set of functions they could perform. An electronic circuit might consist of a CPU, ROM, RAM and other glue logic. The first semiconductor chips held two transistors each. Subsequent advances added more transistors, and as a consequence, more individual functions were integrated over time. The first integrated circuits held only a few devices, perhaps as many as ten diodes, transistors, resistors and capacitors, making it possible to fabricate one or more logic gates on a single device [1].

A digital circuit is often constructed from small electronic circuits called logic gates that can be used to create combinational logic. Each logic gate represents a function of boolean logic. A logic gate is an arrangement of electrically controlled switches, better known as transistors.Counting is a fundamental function of digital circuits. A digital counter consists of a collection of flip-flops that change state (set or reset) in a prescribed sequence. The primary function of a counter is to produce a specified output pattern sequence [2]. A counter can play a vital role in several circuits ranging from a simple display to complex microcontroller circuits. Some of the apparent applications of a counter are: frequency divider in phase-locked loops, microcontrollers, digital memories and in digital clock and timing circuits [3].

Counter is one of the simplest but essential building blocks in very large scale integration design [1,4].Counters are usually classified into synchronous counters, such as up counter ,down counter ,ring counters and twisted counters, and asynchronous counters, such as ripple counter, up counter down counter and Mod N counter.[5] In

synchronous counter a common clock is used which is connected to each flip flop while in asynchronous counter clock is connected to first flip-flop only and the output of one flip-flop derive the input of the next one [6].Synchronous counter has many advantages over asynchronous counter.Asynchronous counter not useful at very high frequencies , especially for counter with large number of bits. Another problem caused by propagation delays in asynchronous counter occurs when we try to electronically detect (decode) the counter's output states.

II. SYNCHRONOUS COUNTER

Synchronous counter is the most popular type of counter. It typically consists of a memory element, which is implemented using flip-flops and a combinational element, which is traditionally implemented using logic gates. Logic gates are logic circuits with one or more input terminals determined by a combination of input signals. The use of logic gates for combinational logic typically reduces the cost of components for counter circuits to an absolute minimum, so it remains a popular approach[3].

The operation of conventional synchronous counters is usually based on a synchronous timing principle in which new data values of the entire counter bits are evaluated at every clock cycle and captured by associated flip-flops (FFs) at every triggering edge of the clock. Because the switching activity of counter bits in a binary counter is decreased by half as the significance of each bit increases, this type of operation apparently causes a lot of redundant transitions, particularly for counter bits having higher significance. Fine-grain clock-gating schemes [7,8] can be used to eliminate these redundant transitions.[9]. For the designing of counter circuit flip flops are used . Flip flops is a storage element based on gated latch principle, which can have its output changed only on the edge of the controlling clock signal. The combination of number of flip flops makes a sequential circuit. The Flip-Flop remains locked on an output of either 0 or 1 until it is given some sequence of inputs, in which case its output will change[10].

Synchronous counter are of two type on the basis of sequence of states i.e. up counter and down counter. In the proposed design of this paper synchronous up counter has been designed using D flip flop. The D flip-flop captures the value of the D-input at a definite portion of the clock cycle (such as the rising edge of the clock). That captured value becomes the Q output. At other times, the output Q does not change. The D flip-flop can be viewed as a memory cell, a zero-order hold, or a delay line. Most D-type flip-flops in ICs have the capability to be forced to the set or reset state (which ignores the D and clock inputs), much like an SR flip-flop. Usually, the illegal S = R = 1 condition is resolved in D-type flip-flops [11].

The designing of synchronous counter first include to draw the state transition diagram showing all the possible states, including those that are not part of the desired counting sequence[12], then use the state transition diagram to set up a table that lists all present states and their nextstates and lastly add a column to this table for flip flop input ,simplify the expression using Karnaugh map. so truth table for synchronous up counter shown in table 1. The proposed synchronous 2-bit up counter has one NOT gates, 1 XOR gates and 2 D flip-flops. Same clock pulse is given to each flip-flop so proposed design is implemented [13].

Table 1: Truth table of 2 Bit Synchronous up Counter

Present state		Next state		Flip flop input	
A	B	A_{n+1}	B_{n+1}	D_A	D_A
0	0	0	1	0	1

0	1	1	0	1	0
1	0	1	1	1	1
1	1	0	0	0	0

III. SCHEMATIC AND LAYOUT

Proposed counter is implemented using DSC 3.1 tool. Transistor level design is implemented using Microwind 3.1 tool. Optimized design is also made by Microwind 3.1. Design of proposed counter 2 bit synchronous up counter using DSCH 3.1 according to the truth table shown in section II can be shown in fig. 1 that is the first schematic design.

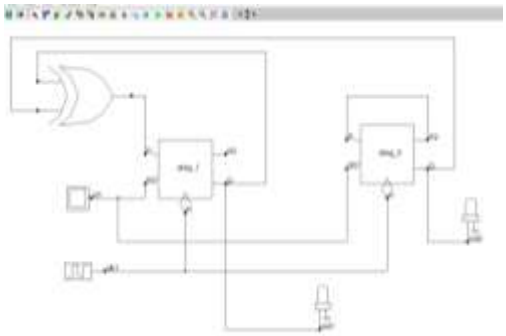


Fig.1: Schematicof 2-Bit Synchronous Up Counter

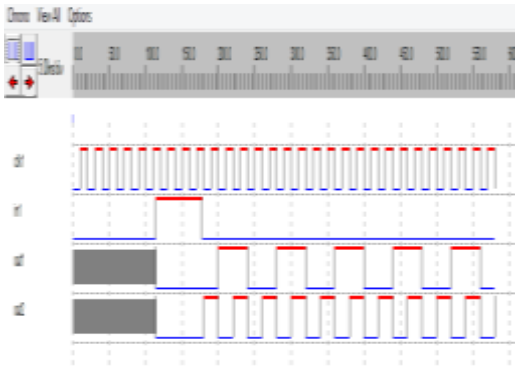


Fig.2:2-Bit Synchronous Up Counter Waveform

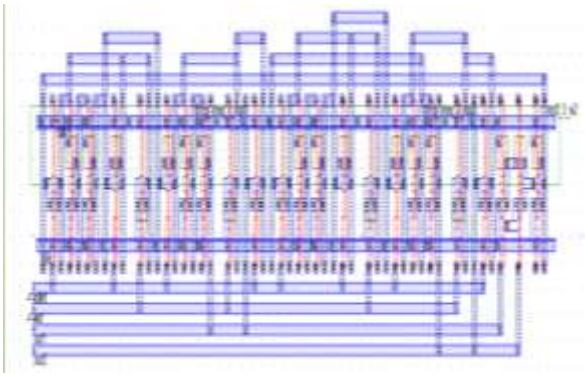


Fig.3: Layout of 2 Bit Synchronous up Counter

The auto generated layout of 2 bit synchronous up counter is obtained by making Verilog file and compile that Verilog file using microwind 3.1 tool. Which is shown in above fig. 3.

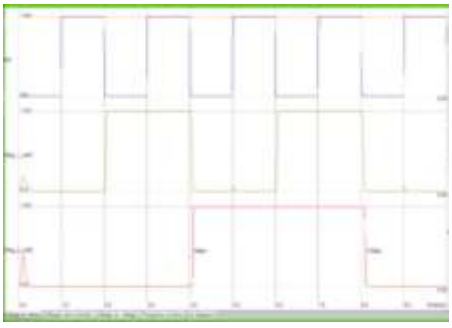
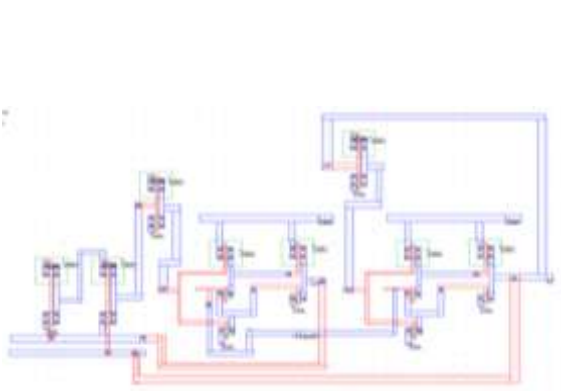


Fig.4: 2 Bit Synchronous up Counter Waveform

Fig.4 shows the output waveform of 2 bit synchronous up counter which is obtained by microwind 3.1 from the autogenerated layout of 2 bit up counter.D flip flop can be made either of transmission gate or by nmos transistor. So For making the area efficient optimized design of 2 bit synchronous up counter 2 layout has been prepared.As 2 bit synchronous up counter is made by d flip flop in this paper ,so in first case layout is made by transmission gate ,which is shown in fig.5. Syncronous up counter which is made by Transmission gate d flip flop is used 18 transistors.



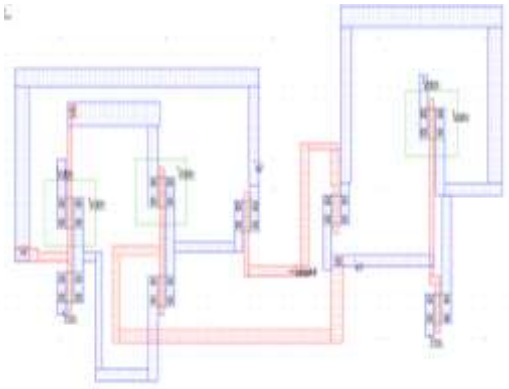


Fig.5:Proposed Layout Using Transmission Gate **Fig.6:Proposed Layout Using NMOS**

D flip flop can also be made using nmos ,so in second case of optimized design of 2 bit synchrnous up counter which is implemented using 8 transistor is shown in fig.6 and the output waveform is shown in fig.7.

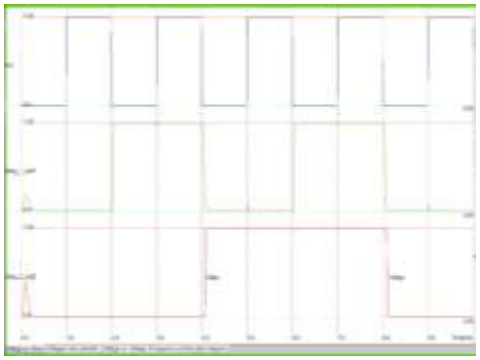


Fig.7:Proposed Layout Output Waveform

IV. RESULT ANALYSIS

As can be seen from the simulated schematic and layout that the auto generated layout is more complex in comparison to the self generated proposed layout. Table 2 shows the performance analysis all three counter on the basis on height, area and power required of each proposed layout and auto generated Layout of 2 bit synchronous up counter.

Table 2 Area and Power Analysis of Two Layout

	Auto generated Layout	Proposed Layout	
		Transmission gate	NMOS
Width	24.1 µm	14.29µm	11.5µm
Height	6.6µm	11.1µm	6.3µm
Area	159.1µm^2	158.7µm^2	76.1µm^2
Power	84.352µW	0.187mW	.153mW

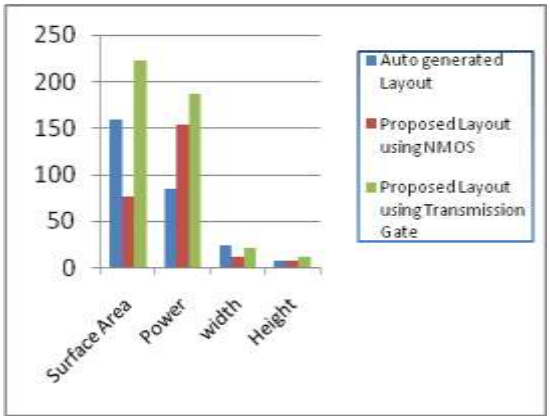


Fig.8: Layout Comparison for Area, Power and Height

The table 2 shows that the consumed power for auto generated layout is 84.352µW that is smaller than the power required for proposed layout, while the surface area requirement of proposed layout in which d flip flop is used as NMOS less in comparison with other two layout .It is also be noticed from all the three layouts that the number of transistor requirement is less in proposed layout which is made by NMOS transistor. Fig.8 shown above is the comparative analysis of auto generated layout and proposed layout and signify which layout perform better.

V. CONCLUSION

This paper includes the design of 2 bit synchronous up counter. Performance analysis of auto generated layout and proposed layout also be done in this paper.For the optimized area efficient proposed layout of synchronous up counter ,2 types of design has been used. one in which D flip flop is made by transmission gate and another one in which D flip flop is made by NMOS.From the result it is clear that optimized proposed layout of synchronous up counter is more area efficient than auto generated layout design .As optimized layout provide 52.16 % less area than the auto generated layout and 52.04% from the layout which used transmission gate as d flip flop. Number of transistor requirement is also less in proposed area efficientoptimized layout.

VI. ACKNOWLDGEMENT

The authors would like to thank Director, National Institute of Technical Teachers' Training & Research, Chandigarh, India for their constant inspirations and support throughout this research work.The authors would also like to thankProf. & Head ECE Department Dr.S.B.LSachan for their worthy guidance and help inwriting this paper.

REFERENCES

[1]. S. Vinoth Kumar and M. Malathi, "Low Power Synchronous Counter Using Improvised Conditional Capture Flip-Flop", Second International Conference on Sustainable Energy and Intelligent System (SEISCON),pp. 589-592 Dr. M.G.R. University, Chennai, Tamil Nadu, India. July. 20-22, 2011.

[2]. N. H. E. Weste and D. Harris, "CMOS VLSI Design", Reading, MA:Pearson Education, Fourth Edition,,pp-379 & 13, 2005.

[3]. A. Ramya, R. Arunya,p. Umaraniand V.Balaamuguran,"Design of Asynchronous up-down, up-down Counter Using power efficient D-Flip Flop", International Journal For Advance Research In Engineering And Technology,Vol. 1 ,Issue 9,pp. 59-63,2013.

[4]. Upwinder Kaur and Rajesh Mehra, "Low Power CMOS Counter using clock gated flip flop",International journal of Engineering and Advanced Technology,VO-2 ,Issue-4,pp-796-798,April ,2013

[5]. YogitaHiremath, Akalpita L. Kulkarni and J. S. Baligar , "Design And Implementation Of Synchronous 4-Bit Up Counter Using 180nm Cmos Process Technology ", International Journal of Research in Engineering and Technology(IJRET) ,Vol 3, Issue 5 ,pp-810-815, May-2014.

[6]. M. R. Stan, A. F. Tenca, and M. D. Ercegovac, "Long and fast up/down counters," IEEE Transaction. Computer, vol. 47, no. 7, pp. 722–735, Jul. 1998.

[7]. Dinesh Sharma and Rajesh Mehra, "Low power,Delay optimized buffer design using 70nm CMOS Technology", International Journal of Computer Application, Vol-22,pp 13-18,May ,2013.

[8]. B.-S. Kong, S.-S. Kim and Y.-H. Jun, "Conditional-Capture flip-flop for Statistical power reduction," IEEE J. Solid-State Circuits, vol.36, no.8, pp.1263–1271, August 2001.

[9]. W. Aloisi and R. Mita, "Gated-clock design of linear-feedback shift registers," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 55, no. 6, pp. 546–550, Jun. 2008.

[10]. Young-Won Kim, Joo-Seong Kim, Jae-Hyuk Oh, Yoon-Suk Park, Jong-Woo Kim,Kwang-Il Park, Bai-Sun Kong, and Young-Hyun Jun , "Low-Power CMOS Synchronous Counter With Clock Gating Embedded Into Carry Propagation",IEEETransactions On Circuits And Systems—II: Express Briefs, Vol. 56, No. 8, pp-649-654,August, 2009.

[11]. Suresh Kumar, "Power And Area Efficient Design of Counter for Low Power VLSI System", International Journal Of Computer Science And Mobile Computing(IJCSMC), Vol. 2, Issue. pp. 435-443, June 2013.

[12]. W. Aloisi and R. Mita, "Gated-Clock Design of Linear-Feedback Shift Registers," IEEE Trans. Circuits Syst. II,Exp. Briefs, vol.55, no.6, pp.546–550, June 2008.

[13]. Upwinder Kaur and Rajesh Mehra, "Optimization of C,OS 8-bit Counter using SLA and Clock Gating Technique" ,International Journal of Recent Technology and Engineering,Vol -3 Issue -5,pp. 44-50 ,July 2013.

AUTHORS

Pragati Guptareceived the Bachelors of Technology degree in Electronics and Communication Engineering from Moradabad Institute of Technology,UPTU, Moradabad, India in 2010, and she is pursuing Masters of Engineering degree in Electronics and Communication Engineering from National Institute of Technical Teachers' Training & Research, Panjab Univsrsity, Chandigarh, India.

Shee is an Assistant Professor with the Department of Electronics & Communication Engineering,, Moradabad Institute of Technology, Moradabad, India. Her current research and teaching interests are in Digital electronics and digital signal processing.

Rajesh Mehra received the Bachelors of Technology degree in Electronics and Communication Engineering from National Institute of Technology, Jalandhar, India in 1994, and the Masters of Engineering degree in Electronics and Communication Engineering from National Institute of Technical Teachers' Training & Research, Panjab Univsrsity, Chandigarh, India in 2008. He is pursuing Doctor of Philosophy degree in Electronics and Communication Engineering from National Institute of Technical Teachers' Training & Research, Panjab Univsrsity, Chandigarh, India.

He is an Associate Professor with the Department of Electronics & Communication Engineering,, National Institute of Technical Teachers' Training & Research, Ministry of Human Resource Development, Chandigarh, India. His current research and teaching interests are in Signal, and Communications Processing, Very Large Scale Integration Design. He has authored more than 175 research publications including more than 100 in journals.