AREA AND POWER EFFICIENT FULL ADDER DESIGN ON 50 NM TECHNOLOGY

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ABSTRACT

Full adder is an important component for the design and development of all types of processors such as digital signal processors (DSPs), microprocessors etc. Adders are the core element of complex arithmetic operations like addition multiplication, division, exponentiation etc. . In most of these systems the adder lies in the critical path that determines the overall performance of the system. In this paper adder has been developed using Gate level, Circuit level. The performance of these different design has been analyzed and compare in term of power, delay, no. of Transistors used and area. The Simulation result show that circit level design is better by 46.78 percent in power and 53.29 percent in delay.

Keywords: Power Dissipation, MOS Devices, Computational Efficiency, Very Large Scale Integration (VLSI), Delay

I. INTRODUCTION

With the explosive growth in laptops, portable personal communication systems, and the evolution of the shrinking technology, the research effort in low-power electronics has been intensified. Today, there are an increasing number of portable applications requiring small-area[1] low-power high throughput circuitry[2,3]. Therefore, circuits with low-power consumption become the major candidates for design of systems. Technology trends show that circuit delay is scaling down by 30%, performance and transistor density are doubled approximately every two years, and the transistor's threshold voltage is reduced by almost 15% every generation. All of these technology trends lead to higher and higher power consumption in circuits. Higher power consumptions raise chips' temperature and directly affect battery life. A higher temperature directly affects circuit operation and reliability; complicated cooling and packaging techniques are required. In addition, higher current density either shortens battery packs .Addition is the most commonly used arithmetic operation in microprocessors and DSPs, and it is often one of the speed-limiting elements . Hence optimization of the adder both in terms of speed and power consumption should be pursued. During the design of an adder we have to make two choices in regard to different design abstraction levels. One is responsible for the adder's architecture implemented with the one-bit full adder as a building block. The other defines the specific design style at transistor level to implement the one-bit full adder. There are several issues related to the full adders. Some of them are power consumption, performance, area, noise immunity and regularity and good driving ability . Several works have been done in order to decrease transistor count and consequently decrease power consumption and area . In some designs, reducing transistor count has been resulted in threshold loss problem that causes non-full swing outputs , low speed and low noise immunity especially when they are used in cascaded fashion. Some of them has threshold loss problem that cause non-full swing outputs, the sentelow

speed and low noise immunity. However, usually they have less power consumption in comparison to full adders with full swing outputs. Not full swing full adders are useful in building up larger circuits as multiple bit input adders and multipliers[4,5]. In Integrated Circuits mainly two types of full adders (Static & dynamic) are used. Static full adders commonly are more reliable, simpler and lower power than dynamic ones. However, dynamic full adders are faster and some times more compact than static full adders. Dynamic full adders suffer from charge sharing, high power due to high switching activity, clock load and complexity.

II. FULL ADDER DESIGN

Gate level schematic of the one bit full Adder: A basic cell in digital computing systems is the 1-bit full adder which has 1-bit inputs (A, B, and C) and two 1-bit outputs (Sum and Carry). The addition of 2 bits (A and B) with input carry C generates the sum bit and the output carry bit. Boolean functions for the two outputs[6] can be manipulated to simplify the circuit as given below:

$$S = ABCin + AB'C'in + A'B'Cin + A'BC'in \quad (1)$$

$$Cout = AB + ACin + BCin \quad (2)$$

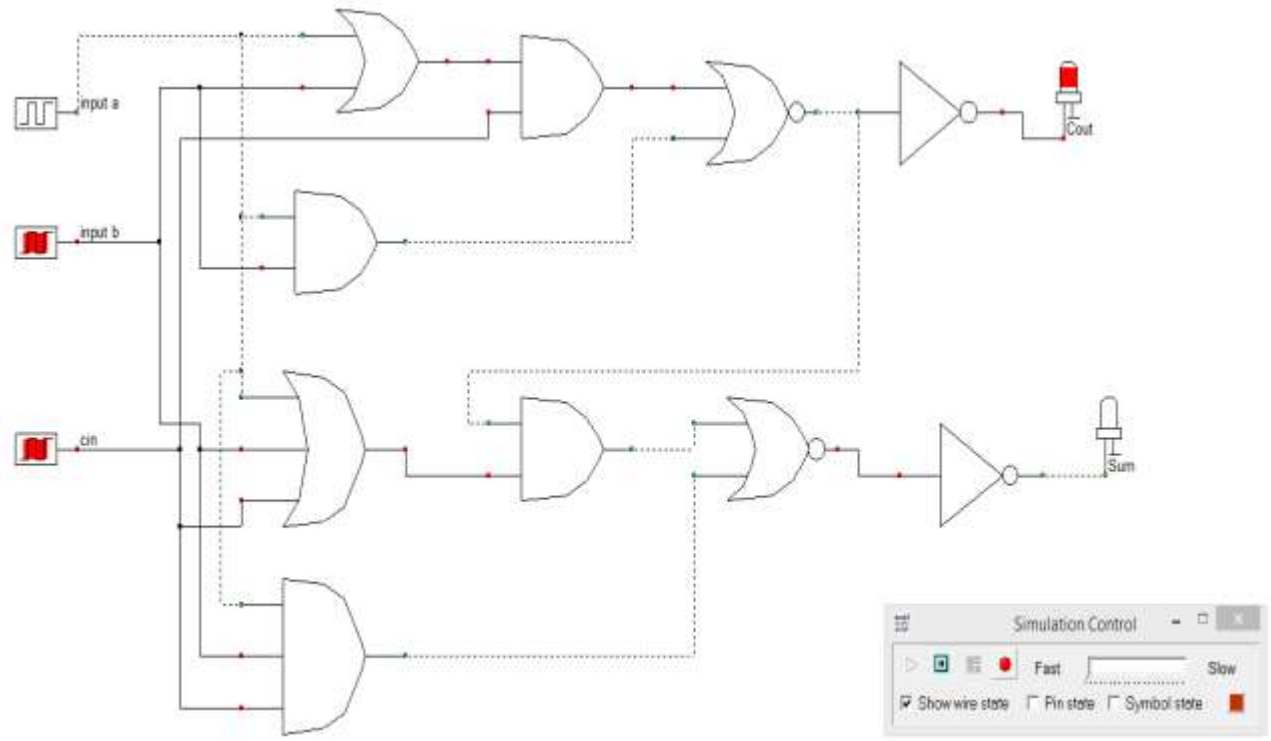

Fig. 1 Gate level schematic of the full Adder

Full Adder Using Two Half Adder: A full adder can be constructed from two half adders by connecting A and B to the input of one half adder, connecting the sum from that to an input to the second adder, connecting Ci to the other input and OR the two carry outputs[9,10]. The critical path of a full adder runs through both XOR-gates and ends at the sum bit S.

Table.1 Truth Table of full adder

X	Y	C_{IN}	SUM	C_{OUT}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

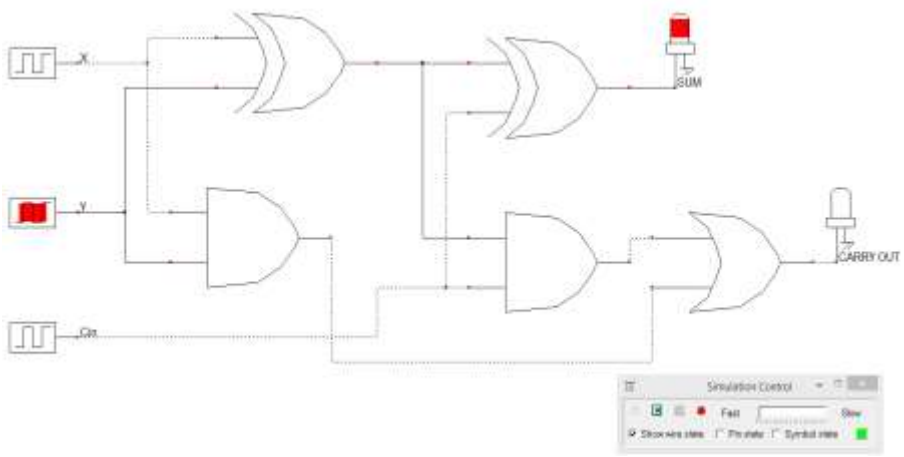

Fig.2 Full Adder using two half Adder

Static energy recovery Full Adder: In this type of adder the energy recovering logic reuses charge and therefore consumes less power than non-energy recovering logic.[7,8]

Working principle: The circuit consists of two XNORs realized by 4 transistors. Sum is generated from the output of thesecond stage XNOR circuit. The cout can be calculated by multiplexing a and cin controlled by (a ⊗ b). Let us consider that there is a capacitor at the output node of the first XNOR module. To illustrate static energy recovery let us consider an example where initially a=b=0 and then a changes to 1. When a and b both equals to zero the capacitor is charged by VDD. In the next stage when b reaches a high voltage level keeping a fixed at a low voltage level,the capacitor discharges through a. Somecharge is retained in a. Hence when a reaches a high voltage level we do not have to charge it fully. So the energy consumption is low here[10,11].

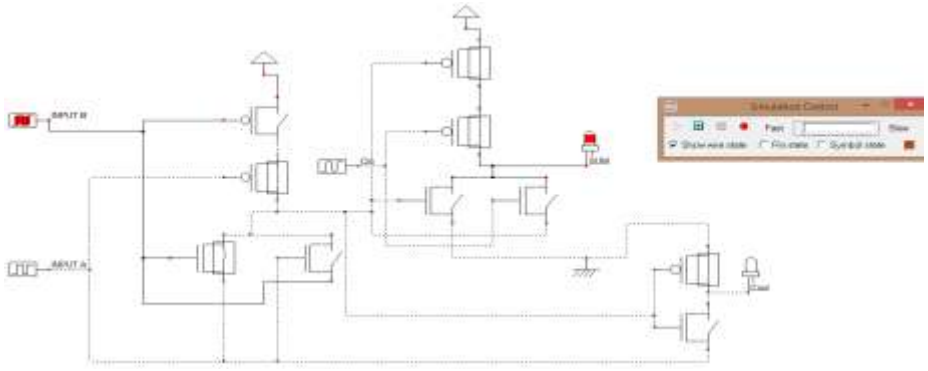

Fig.3 SERF Full Adder

Full adder with XOR and 2:1 Multiplexers : Hence Sum can be implemented using two XOR gates. Carry can be implemented using a 2:1 multiplexer with A and CIN as input lines and X as selection line.

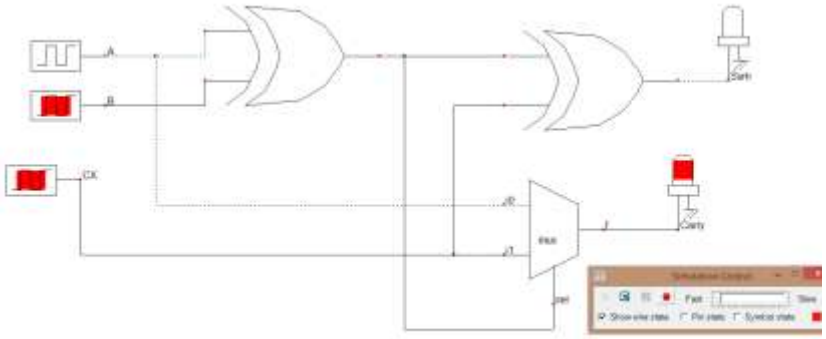

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Fig. 4 Full adder with XOR and 2:1 Multiplexer

1-bit full adder using Two XNOR gates and one 2:1 Mux: Here Sum can be implemented using two XNOR gates. Carry can be implemented using a 2:1 multiplexer with A and CIN as input lines and X‘ as selection line

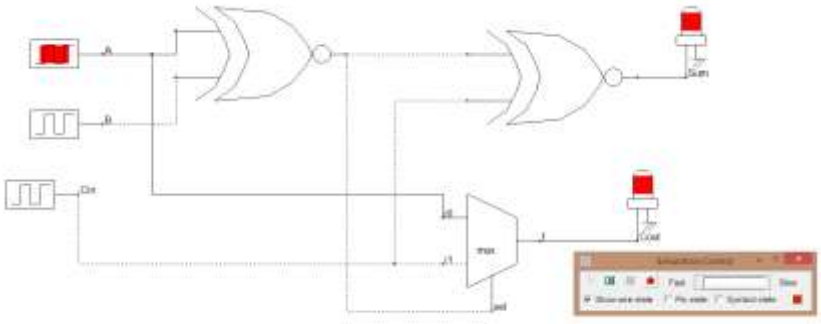

Fig. 5. Full adder with XONR and 2:1 Multiplexer

III. FULL ADDER LAYOUT SIMULATION

3.1 Logic Level Full Adder Implementation

The DSCH program is a logic editor and simulation .It provides user-friendly an fast simulation. Full adder using gates is implemented on DSCH[5] then its verilog file is generated and its layout and simulated result shown in Fig. below. It has been observe that for Gate level schematic of the full Adder average power

consumption is 55.064 µw, area is 116.8 µm2 Delay is found to be 0.283 ns and no transistor used is 26 Pmos and 26 Nmos.

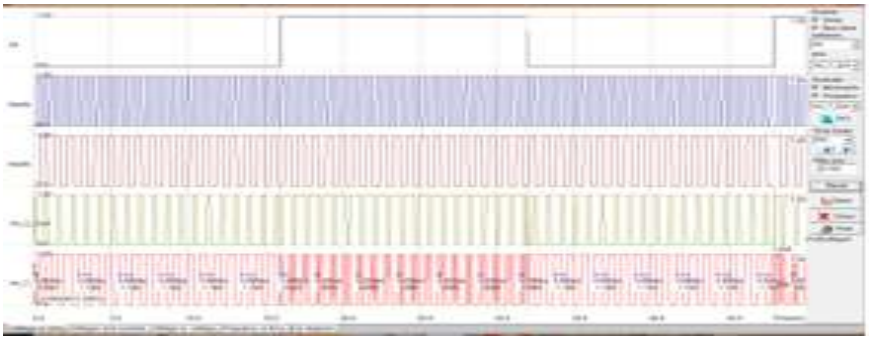

Fig. 6. Simulation Result of Gate Level Schematic of The Full Adder

Fig. 7 Layout of Gate Level Schematic of The Full Adder

3.2 Full Adder Using Two Half Adder

It has been observe that for Gate level schematic of the one bit full Adder average power consumption is 64.370 µw, area is 67.9 µm2 Delay is found to be 0.955 ns and no transistor used is 15 Pmos and 15 Nmos.

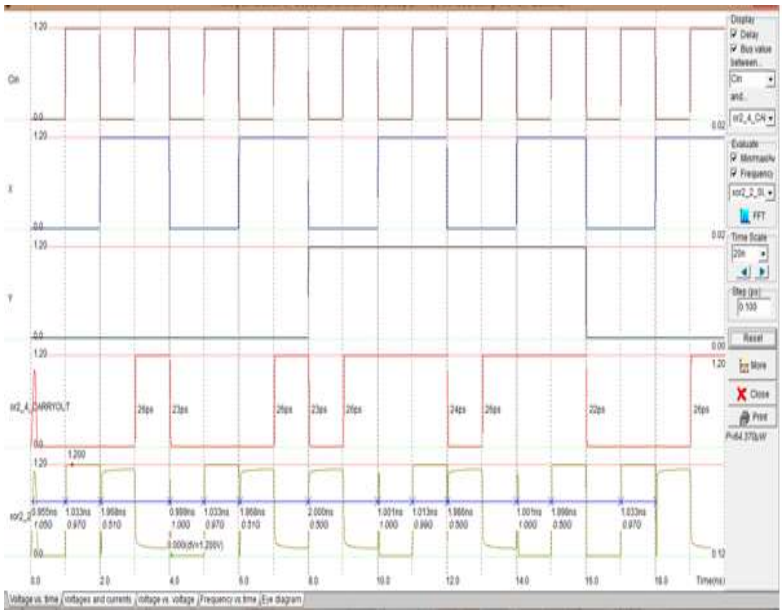

Fig. 8 Simulation Result Full Adder Using Two Half Adder

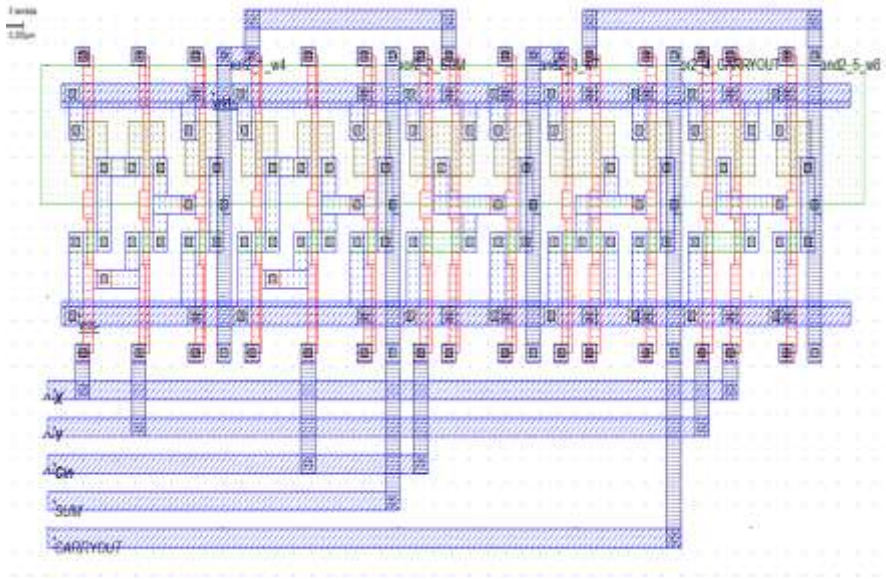

Fig. 8 Layout of Full Adder Using Two Half Adder

3.3 Circuit Level Full Adder Implementation

Static energy recovery Full Adder: It has been observe that for circuit level schematic of the one bit CMOS full Adder average power consumption is 34.252µw, area is 80 µm2 Delay is found to be 0.446 ns and no transistor used is 5 Pmos and 5 Nmos.

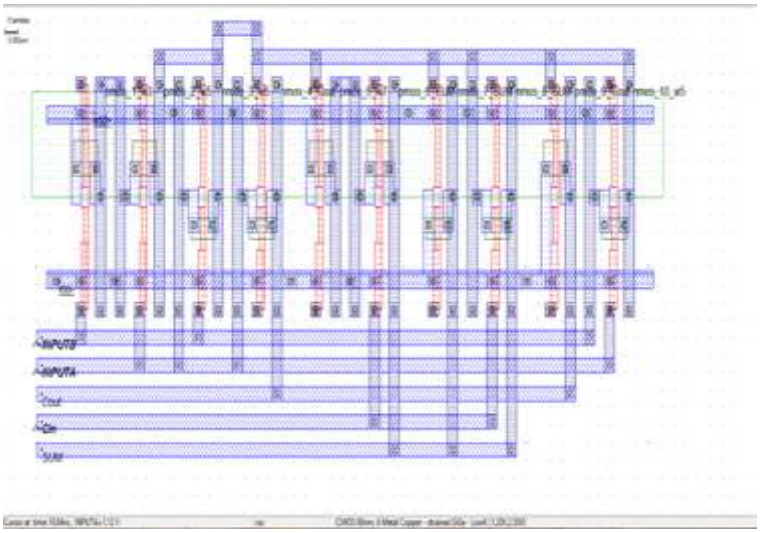

Fig. 9. Layout of Static energy recovery Full Adder:

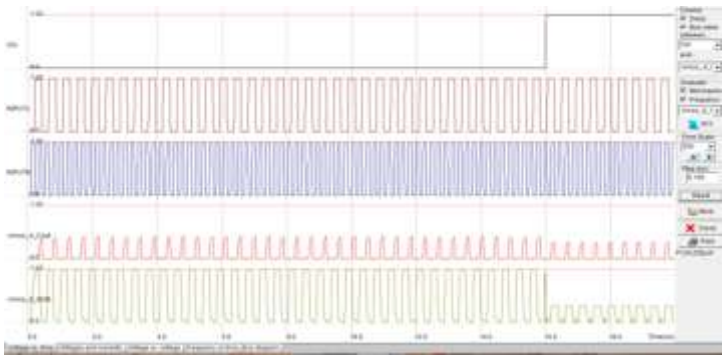

Fig. 10 Simulation result of Static energy recovery Full Adder

3.4 Full Adder with XOR And 2:1 Multiplexer

Full adder with XOR and 2:1 Multiplexers : It has been observe that for Hybrid level schematic of the full Adder average power consumption is 52.035µw, area is 74.6 µm2 Delay is found to be 8 ns and no transistor used is 9 Pmos and 9 Nmos.

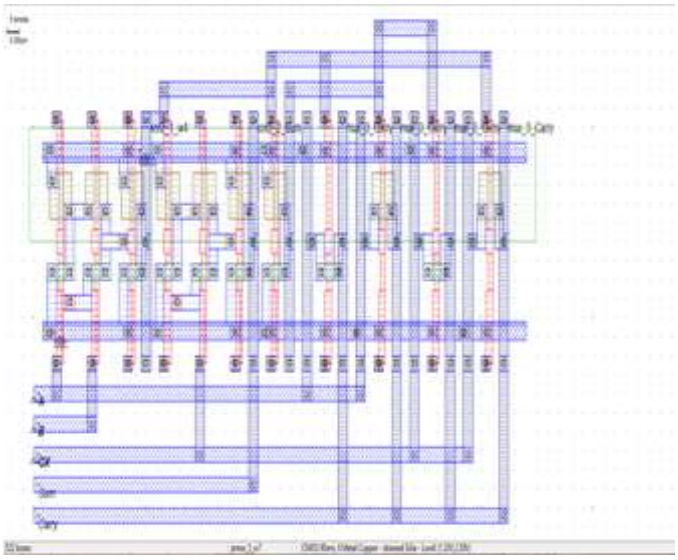

Fig. 11 Layout of of 1-bit Full adder with XOR and 2:1 Multiplexers

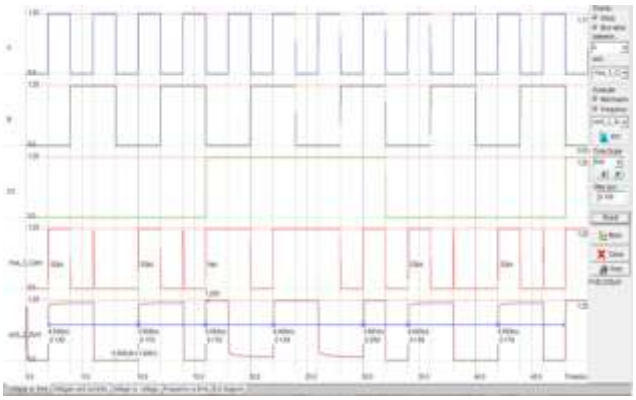

Fig. 12 Simulation result of 1-bit Full adder with XOR and 2:1 Multiplexers

Full adder with XNOR and 2:1 Multiplexers : It has been observe that for Hybrid level schematic of the one bit full Adder average power consumption is 52.035µw, area is 74.6 µm2 Delay is found to be 8 ns and no transistor used is 9 Pmos and 9 Nmos.

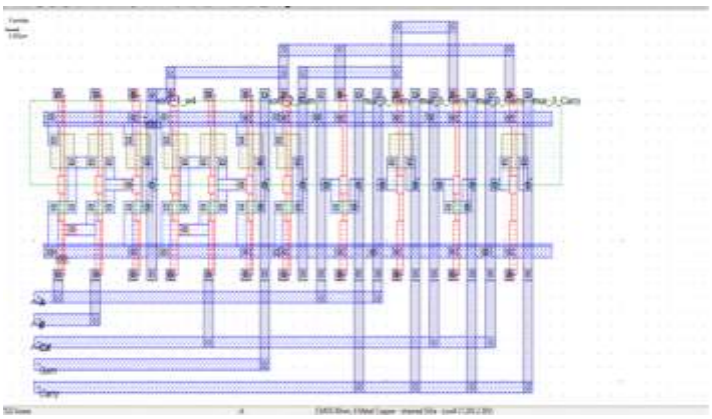

Fig. 13 Layout of of 1-bit Full adder with XOR and 2:1 Multiplexers

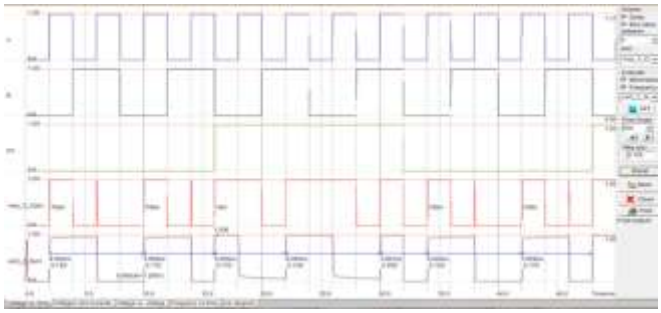

Fig. 14 Simulation result of 1-bit Full adder with XNOR and 2:1 Multiplexers

IV. RESULT ANALYSIS

Comparative analysis between various type of Full Adder is shown in Fig: No. of transistor is very less in Static energy recovery Full Adder as compared to gate level implementation. delay is maximum in Full adder with XOR and 2:1 Multiplexers and Full adder with XNOR and 2:1 Multiplexers, Gate level schematic of the full Adder has maximum no. of transistor.

Table.1 Comparative analysis of various type of Full Adder

S no.	FULL ADDER CIRCUIT	P (µW)	AREA (μm^2)	DELAY (ns)	NUMBER OF TRANSISTER
1.	Gate level schematic of the full Adder	**55.064**	116.8	0.283	26 nmos 26 pmos
2.	Full Adder Using Two Half Adder	**64.370**	67.9	0.955	15 nmos 15 pmos
3.	Static energy recovery Full Adder	**34.252**	80.0	0.446	5 nmos 5 pmos
4.	Full adder with XOR and 2:1 Multiplexers	**52.035**	74.6	8.000	9 nmos 9 pmos
5.	Full adder with XNOR and 2:1 Multiplexers	**52.035**	74.6	8.000	9 nmos 9 pmos

V. CONCLUSION

From the analysis of the above various type of Full Adder Circuits we can reach to a conclusion that the average power is low, area is increased to some extent and Power Delay Product is also low for Static energy recovery Full Adder among all types of adder. No. of transistor is very less in Static energy recovery Full Adder as compared to gate level implementation. For Optimization of Power (Average power) and Delay, we think that the best option is Static energy recovery Full Adder .

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