DESIGN ANALYSIS OF AREA EFFICIENT 4 BIT SHIFT REGISTER USING CMOS TECHNOLOGY

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ABSTRACT

In this paper a detailed area and power analysis of 4- bit shift register is carried out. Three methods are compared in terms of area and the method with least area requirement is suggested for the design. First method is by using DSCH software followed by generating the Verilog file and then compiling the same in Microwind software. The result will be an auto generated circuit of 4- bit shift register. The circuit is then simulated and the area is measured. Second method follows the implementation of 4 bit shift register using Microwind software by using the available P-MOS and N-MOS in the software. Circuit is simulated and the power is measured again. Third method involves the implementation of the circuit by generating our own N-MOS and PMOS transistors and then simulating the circuit and then measuring the area and then the final comparison of all is done.

Key Words: 4 bit shift register-P-MOS, N- MOS, flip flop, semiconductors

I.INTRODUCTION

The rapid growth in semiconductor device industry has led to the development of high performance portable systems with enhanced reliability [1]. In such portable applications, it is extremely important to minimize area [2] and current consumption due to the limited availability of battery power [1]. Therefore,area utilization,power dissipation becomes an important design issue in VLSI circuits[4][5].

In digital circuits, a shift register is a cascade of flip flops, sharing the same clock, in which the output of each flip-flop is connected to the "data" input of the next flip-flop in the chain, resulting in a circuit that shifts by one position the "bit array" stored in it, shifting in the data present at its input and shifting out the last bit in the array, at each transition of the clock input. More generally, a shift register may be multidimensional, such that its"data in" and stage outputs are themselves bit arrays. This is implemented simply by running several shift registers of the same bit-length in parallel. Shift registers can have both parallel and serial inputs and outputs. These are often configured as 'serial-in, parallel-out' (SIPO) or as 'parallel-in serial-out' (PISO). Shift registers produce a discrete delay of a digital signal or waveform. A waveform synchronized to a clock, a repeating square wave, is delayed by "n" discrete clock times where "n" is the number of shift register stages. Thus, a four stage shift register delays "data in" by four clocks to "data out". The stages in a shift register are delay stages, typically type "D" Flip-Flops or type "JK" Flip-flops. Formerly, very long (several hundred stages) shift registers served as digital memory. This obsolete application is reminiscent of the acoustic mercury delay lines used as early computer memory [6]. Serial data transmission, over a distance of meters to kilometres, uses shift registers to convert parallel data to serial form. Serial data communications replaces many slow parallel data wires with a single serial high speed circuit.

Some specialized counter circuits actually use shift registers to generate repeating waveforms. Longer shift registers, with the help of feedback generate patterns so long that they look like random noise, pseudo-noise.The suggested methods in this paper can be implemented for linear feedback shift registers [6] and in counters also. Basic shift registers are classified [7]by structure according to the following types:

- Serial-in to Parallel-out (SIPO) - The register is loaded with serial data, one bit at a time, with the stored data being available at the output in parallel form.
- Serial-in to Serial-out (SISO) - The data is shifted serially "IN" and "OUT" of the register, one bit at a time in either a left or right direction under clock control.
- Parallel-in to Serial-out (PISO) - The parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.
- Parallel-in to Parallel-out (PIPO) - The parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse.

II.SHIFT REGISTER-WORKING

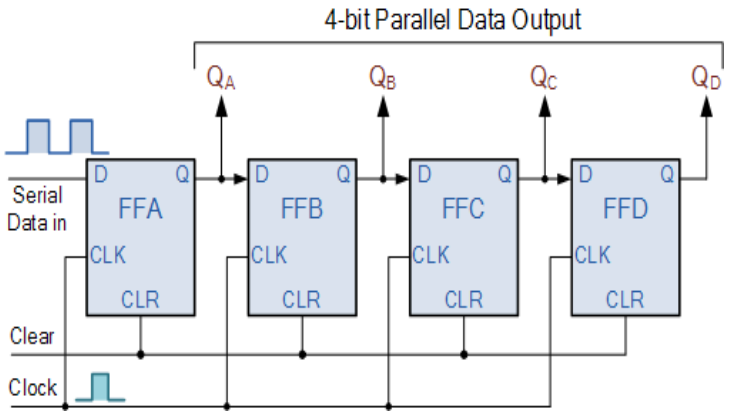

Fig1. 4-bit Serial-in to Parallel-out Shift Register[7].

The operation is as follows. Let's assume that all the flip-flops (FFA to FFD) have just been RESET (CLEAR input) and that all the outputs Q_A to Q_D are at logic level "0" i.e., no parallel data output. If a logic "1" is connected to the DATA input pin of FFA then on the first clock pulse the output of FFA and therefore the resulting Q_A will be set HIGH to logic "1" with all the other outputs still remaining LOW at logic "0". Assume now that the DATA input pin of FFA has returned LOW again to logic "0" giving us one data pulse or 0-1-0.

The second clock pulse will change the output of FFA to logic "0" and the output of FFB and Q_B HIGH to logic "1" as its input D has the logic "1" level on it from Q_A. The logic "1" has now moved or been "shifted" one place along the register to the right as it is now at Q_A.When the third clock pulse arrives this logic "1" value moves to the output of FFC (Q_C) and so on until the arrival of the fifth clock pulse which sets all the outputs Q_A to Q_D back again to logic level "0" because the input to FFA has remained constant at logic level "0".

The effect of each clock pulse is to shift the data contents of each stage one place to the right, and this is shown in the following table until the complete data value of 0-0-0-1 is stored in the register. This data value can now be read directly from the outputs of Q_A to Q_D.Then the data has been converted from a serial data input signal to a parallel data output. The truth table and following waveforms show the propagation of the logic "1" through the register from left to right as follows.

	CLK	$D_n = Q_3$	$Q_3 = D_2$	$Q_2 = D_1$	$Q_1 = D_0$	Q_0
Initially			0	0	0	0
(i)	↓	1	1	0	0	0
(ii)	↓	1	1	1	0	0
(iii)	↓	1	1	1	1	0
(iv)	↓	1	1	1	1	1

→ Direction of data travel

Table1. Basic Data Movement through A Shift Register

Note that after the fourth clock pulse has ended the 4-bits of data (0-0-0-1) are stored in the register and will remain there provided clocking of the register has stopped. In practice the input data to the register may consist of various combinations of logic "1" and "0".

III. ANALYSIS OF LAYOUT USING THREE DIFFERENT TECHNIQUES

The first method is the designing of the ring counter in DSCH and generating its Verilog file. Now in Microwind this Verilog file is compiled and an autogenerated layout is created. We can select different foundries available in the library of Microwind software. Here the selected foundry is 90 nm. Figure2 represents this auto generated layout.

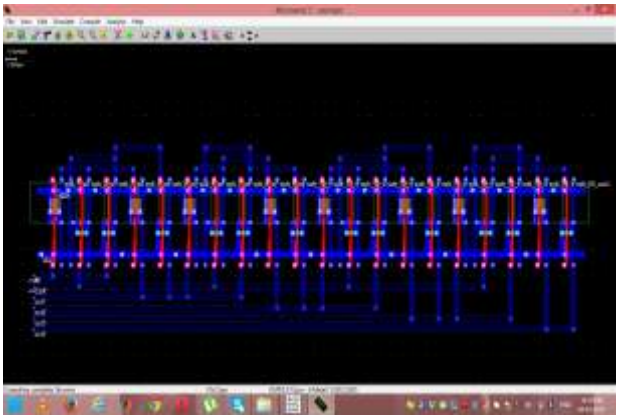

Figure 2. Auto Generated 4 bit shift register

This layout is checked for DRC and if there is no errorpresent in the layout then the layout is simulated. Theoutput of the simulation is checked and if the outputmatches the output of the 4 bit shit registerthen wefurther check the power and the area of this auto generated layout of 4- bit shift register. Figure 3 showsthe output of the 4 bit shift register. Also power canbe measured from the result of simulation.

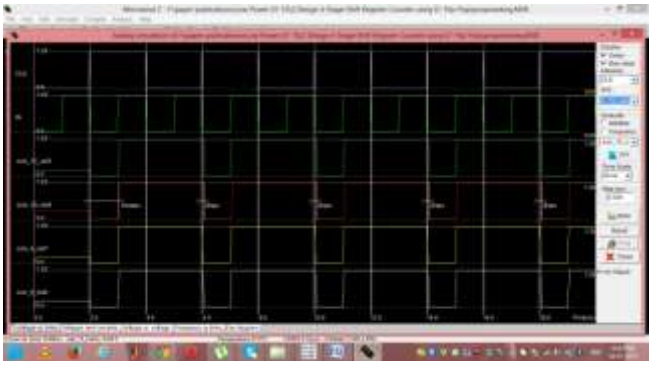

Figure 3. Output of Auto Generated 4 bit shift register

The measured power here is 10.725µW. The area consumed here is 251.1µm^2.Now the second step is to directly make use of in built transistors available in the Microwind software.In this method the connections are made by thedeveloper and hence there is a large possibility thatarea may get reduced. Figure 4 represents the layoutusing the in- built transistors i.e. N- MOS and PMOS.

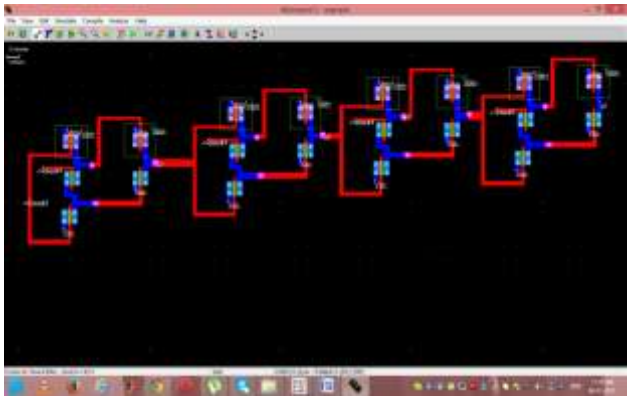

Figure 4. Layout of 4 bit shit register with in- built transistors

When the layout is ready it is again checked for DRCand if there is no error present in the layout, the circuitis simulated and the outputs are obtained. Theobtained output is verified with the truth table of 4 bit shift register. If the truth table is verified we canfurther check the power and area consumed by thissecond method. Figure 5 shows the output obtained bysimulating the above circuit.

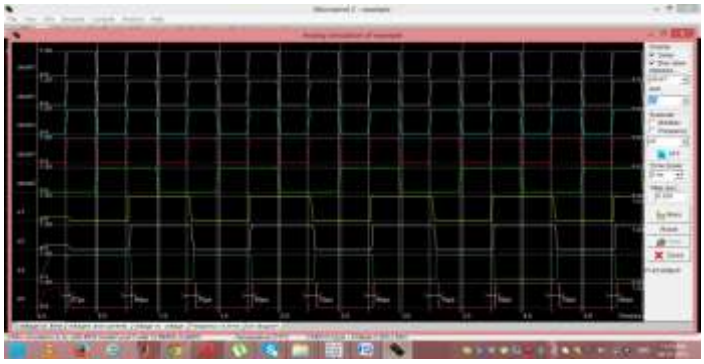

Figure 5.Outputs of 4 Bit Shift Register Using In- Builttransistors

Now check the results for power and area. Here thepower consumed is 24.003 µW. The area consumed bythis layout is 203.0 µm^2.The third method is to create our own N- MOS and PMOStransistors. Here the created transistors are made using palette. Here the area measured is 183.8µm.

This new layout is shown in figure 6.

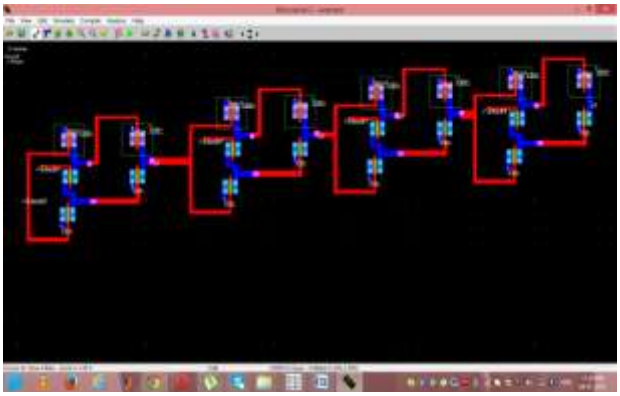

Figure 6. Layout of 4 Bit Shift Register Using Own Created NMOSAND P-MOS

IV. COMPARATIVE ANALYSIS

A comparative study can be done on analyzing the above results for power and area obtained by using three different methods.

TABLE 2: Comparative analysis of Power and Area

METHODS	POWER	AREA
Auto Generated Layout	10.725 µW	251.1µm^2
Layout using in-built transistors	24.003 µW	203.0µm^2
Layout using own created transistors	.279 mW	183.8µm^2

comparative analysis of this table shows that in terms of power, the layout generated using in- built transistors are increasing. But on the other hand in terms of area the auto generated layout is using more area in comparison to the layout using in- built transistors and the self created transistors. There is a reduction of 19.15% in area when auto generated layout is compared to layout using in- built transistors. When auto generated layout is compared to layout using self created transistors then there is a reduction of 26.8% in the area. Now when both the layout with inbuilt and self created transistors is compared in terms of area then there is a reduction of 9.4% in the area.

V. CONCLUSION

From the above analysis it can be said that the layout with self created transistors is more efficient in terms of area. So this design can be implemented in the applications where area reduction is the main consideration. Hence area is decreased at the cost of power. So it can be efficiently used for applications requiring minimum area.

VI. ACKNOWLEDGEMENT

The authors would also like to thank Director, National Institute of Technical Teachers‟ Training &Research, Chandigarh, India for their support during work.

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