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CO JOINING OF COMPRESSOR ADDER WITH 8x8 BIT VEDIC MULTIPLIER FOR HIGH SPEED

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ABSTRACT

In this paper we present technique of 'Co joining of compressor adder with 8x8 bit Vedic multiplier for high speed'. Vedic mathematics is an ancient technique for solving the complex problems. Equations of each 16 bit resultant are calculated using Urdhava-triyakbhyam sutra in English named as 'Vertically and Crosswise' technique. The best feature of this method is that the partial product needed for the multiplication are already generated in advance and this lead to decrease in delay and thus saves time. Compressor adders are used to implement these equations. In comparison to traditional architectures of compressor using half and full adders the modified compressor adder that make use of MUX gave better delay performance. Designs are coded in VHDL and synthesis in Xilinx ISE 14.5 with Spartan 3e series of FPGA, fg320 and speed grade -4.

Keywords: Vedic Mathematics, Urdhava-Triyakbhyam Method, Compressor Adder.

I. INTRODUCTION

These days we have concern about three main issues in VLSI domain i.e. Speed, Area, Power and these all are related with microprocessor and the speed is utmost need everywhere, the speed of the processor merely depends on how it is performing multiplications as all data processing needs multiplication so multiplication is the building block that describes the speed. The equations of 16 bit resultant are calculated using Urdhava-Triyakbhyam method which is an ancient sutra derived from Vedas. Compressor adder are used to implement them Basically we have two types of compressor adder in the purposed methodology one are traditional that make use of compressor adder made up of half adders and full adders only and other are modified compressor adder that make use of compressor adder that are made of half adder and full adder from multiplexers. Compressor adders used with Mux perform better delay performance as compares to traditional ones. Urdhava-Triyakbhyam method for two eight bit numbers is given below:

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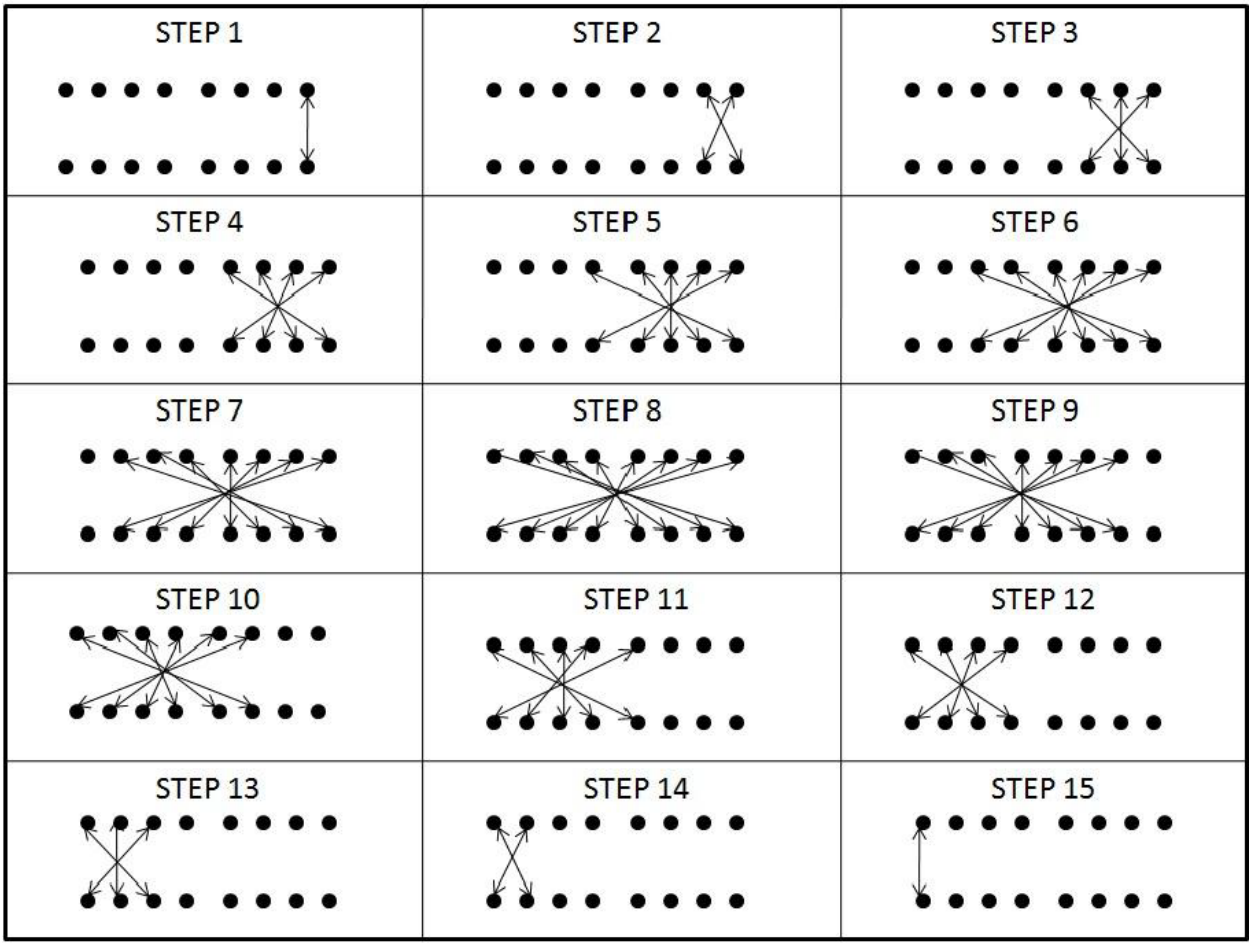

FIGURE 1: Pictorial representation of Urdhva-Tiryakbhyam Sutra for multiplication of two eight bit numbers

This paper compromises of four sections. Section I describes Introduction. Section II compressor adders. Section III is implementation and equations. Section IV Tables and simulation results. Section V Conclusion and future scope.

II. COMPRESSOR ADDER

Compressor adders are basic circuits which add bits more than four at a time to give better delay. The symbolic representation of compressor architecture is $N{-}r$ where 'N' represents the number of the bits that are fed and 'r' represents the total count of the1s present in N bits.

2.1. 2-2 compressor adder: A 2-2 compressor adder is a logical circuit in which maximum two bits can be added at same time and two bit resultant can be obtained. The circuit is simply a half adder. Fig2. represent modified 2-2 compressor adder that uses half and full adder made up from 2:1 MUX.

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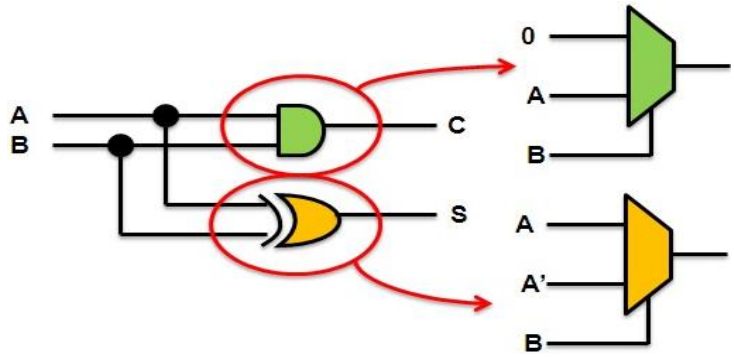

FIGURE2. Modified Design of Half Adder

2.2. 3-2 compressor adder: A 3-2 compressor adder is a logical circuit in which maximum three bits can be added at same time and two bit resultant can be obtained. The circuit is simply a full adder. Fig3. represent modified 3-2 compressor adder that uses half and full adder made up from 2:1 MUX.

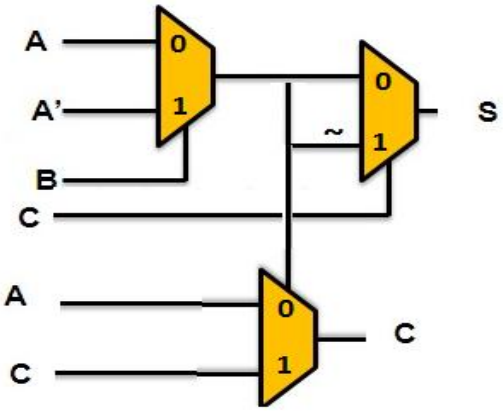

FIGURE3. Modified Design of Full Adder

2.3. 4-3 compressor adder: A 4-3 compressor adder is a logical circuit in which maximum four bits can be added at same time and three bit resultant can be obtained. The half adder and full adder designs with the use of multiplexers mentioned before are being used in a modified designed.

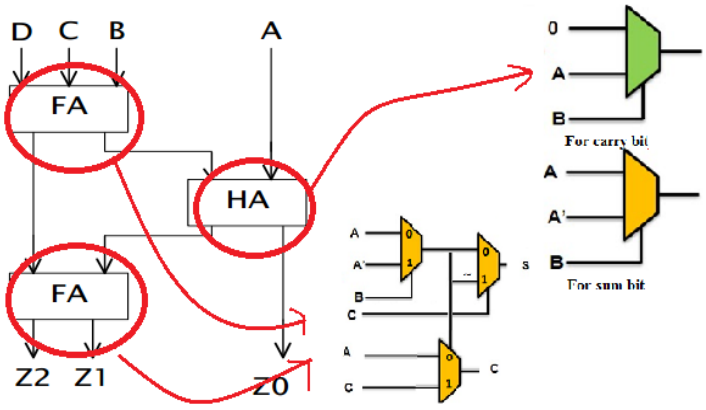

FIGURE4. Modified Design of 4-3 compressor Adder

2.4. 5-3 compressor adder: A 5-3 compressor adder is a logical circuit in which maximum five bits can be added at same time and three bit resultant can be obtained. The half adder and full adder

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designs with the use of multiplexers mentioned before are being used in a modified designed. If we are considering all the inputs to be 1 then the maximum output can be 101.

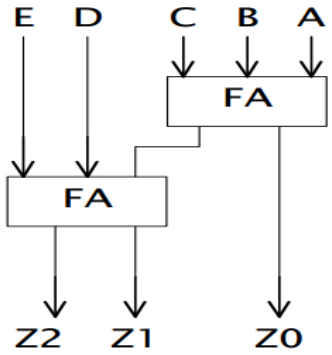

FIGURE5. Modified Design of 5-3 compressor Adder

2.5. 6-3 compressor adder: A 6-3 compressor adder is a logical circuit in which maximum six bits can be added at same time and three bit resultant can be obtained. The half adder and full adder designs with the use of multiplexers mentioned before are being used in a modified designed.

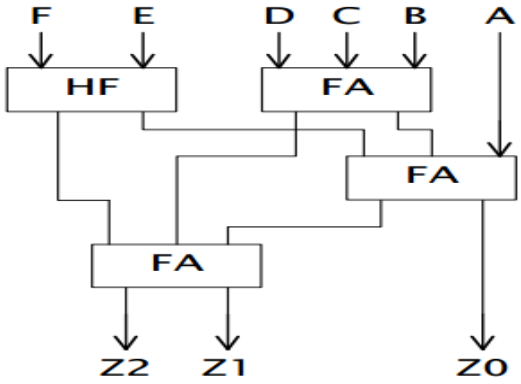

FIGURE6. Modified Design of 6-3 compressor Adder

2.6. 7-3 compressor adder: A 7-3 compressor adder is a logical circuit in which maximum seven bits can be added at same time and three bit resultant can be obtained. The half adder and full adder designs with the use of multiplexers mentioned before are being used in a modified designed.

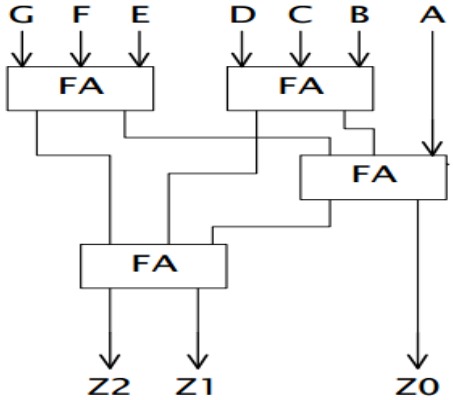

FIGURE7. Modified Design of 7-3 compressor Adder

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2.7. Purposed compressor adder for N=10

The model which is purposed i.e. given above as here N=10 therefore it can take any value till N=10 and give us output as according to it. If we talk about 1st equation it is simply and gate operation and initially as there is no carry so carry bit will remain zero then next in 2nd equation 2-2 compressor adder will be used i.e. simply a half adder it will have two inputs i.e. A_1B_0 and B_0A_1 and will give one sum bit i.e. S_0 and one carry bit C_1. In next equation 4-3 compressor adder will be used it will have four inputs A_0B_2, A_1B_1, A_2B_0 & previous carry C_1 and give output as one sum bit S_2 and two carries bit C_2 & C_3 For next equation 5-3 compressor adder will be used and so on the compressor adders will be used as per the input and give result according to it.

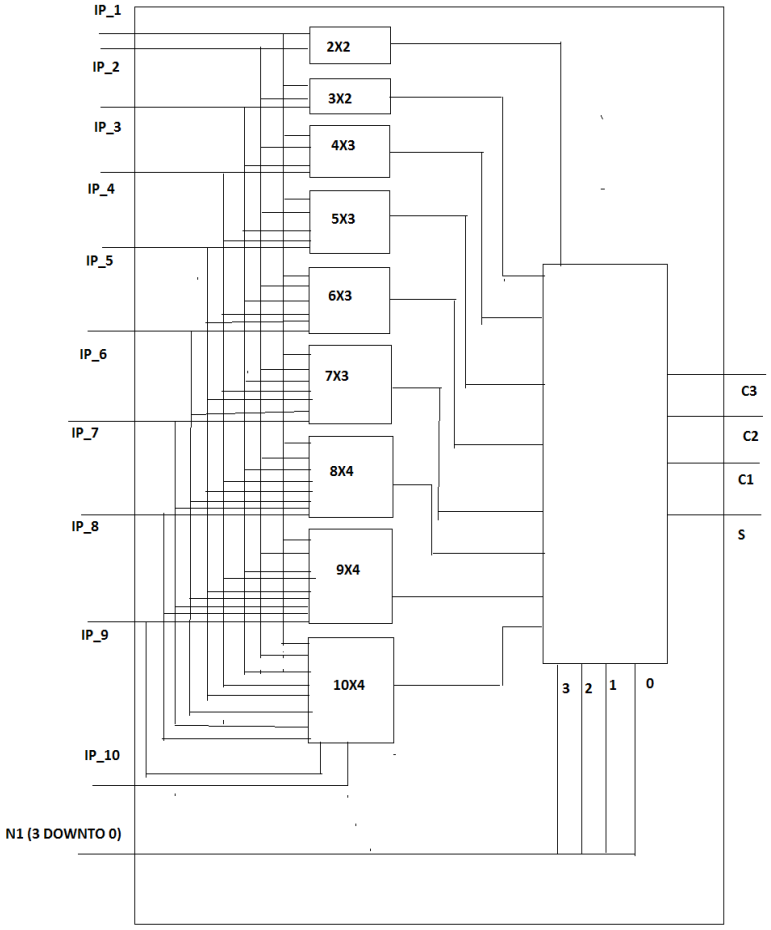

FIGURE8. Purposed compressor adder for N=10

III. EQUATIONS TO BE IMPLEMENTED

Let two 8 bit numbers be

$A= A_0A_1A_2A_3A_4A_5A_6A_7$

$B=B_0B_1B_2B_3B_4B_5B_6B_7$

Now the Resultant bits R = (0-15)

Carry bits C = (C_1- C_{32})

S0 : A0B0

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C1 S1 : A1B0 + B0A1

C3 C2 S2 : C1 + A0B2 + A1B1 +A2B0

C5 C4 S3 : C2 + A0B3 + A1B2 + A2B1 + A3B0

C7 C6 S4 : C3 + C4 + A0B4 + A1B3 + A2B2 + A3B1 + A4B0

C10 C9 C8 S5 : C5 + C6 + A0B5 + A1B4 + A2B3 + A3B2 + A4B1 + A5B0

C13 C12 C11 S6 : C7 + C8 + A0B6 + A1B5 + A2B4 + A3B3 + A4B2 + A5B1 + A6B0

C16 C15 C14 S7 : C9 + C11 + A0B7 + A1B6 + A2B5 + A3B4 + A4B3 + A5B2 + A6B1 + A7B0

C19 C18 C17 S8 : C10 + C12 + C14 + A1B7 + A2B6 + A3B5 + A4B4 + A5B3 + A6B2 + A7B1

C22 C21 C20 S9 : C13 + C15 + C17 + A2B7 + A3B6 + A4B5 + A5B4 + A6B3 + A7B2

C25 C24 C23 S10 : C16 + C18 + C20 + A3B7 + A4B6 + A5B5 + A6B4 + A7B3

C27 C26 S11 : C19 + C21 + C23 + A4B7 + A5B6 + A6B5 + A7B4

C29 C28 S12 : C22 + C24 + C26 + A5B7 + A6B6 + A7B5

C31 C30 S13 : C25 + C27 + C28 + A6B7 + A7B6

C32 S14 : C29 + C30 + A7B7

C33 S15 : C31 + C32

IV. RESULTS

The designs are coded in VHDL and synthesized using Xilinx ISE 14.6 simulator and family used is XILINX: SPARTAN 3E:XC3S500E FG3200, speed grade -4. Results are clearly indicating better speed performance. Table 1 is tabulated with the comparison results of combinational delay of 8 bit multiplier on basis of with use of multiplexers or not using multiplexers Table 2 is tabulated with the comparison results of combinational delay of modified compressor adder with traditional ones. Table 3 is tabulated with results of Combinational delay of Dedicated and General 8 bit Multiplier for N=10.

Multiplier	Combinational delay(ns)	
	Without use Of Multiplexers	With use of Multiplexers
8	16.630	14.317

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FIGURE 9.Comparison table of 8 bit multiplier with use of MUX or without use of MUX

Input bits	Combinational delay(ns)		Percentage improvement (%)
	Modified Comp Results of Yogita_b	Modified comp result of purpsd adders	
2		0.670	
3		0.755	
4		0.788	
5	5.570	0.874	84.308
6		0.882	
7		1.352	
8		1.363	
9		2.545	
10	6.787	1.476	78.252

FIGURE 10. Comparison table of combinational delay for modified compressor adder of base paper and purposed compressor adders

Multiplier	Combinational delay(ns)	
	Dedicated 8 bit Multiplier For N=10	General 8 bit Multiplier For N=10
8	12.270	14.317

FIGURE 11. Comparison table of 8 bit multiplier as a dedicated 8 bit multiplier and as a general 8 bit multiplier for N=10

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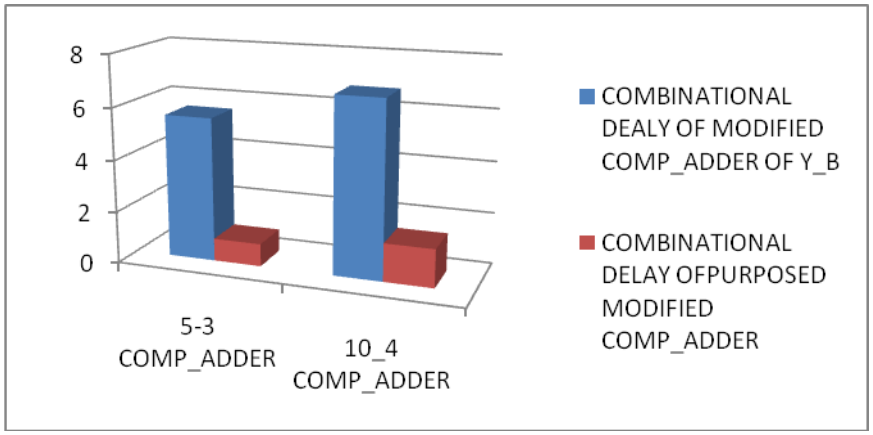
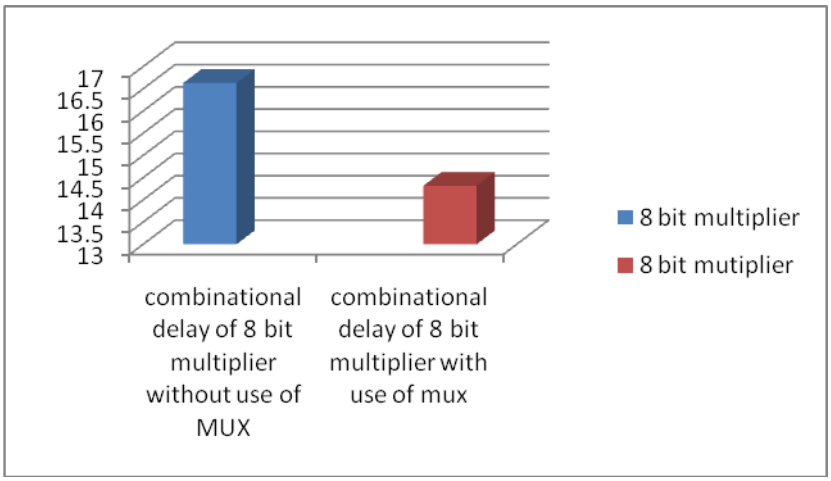
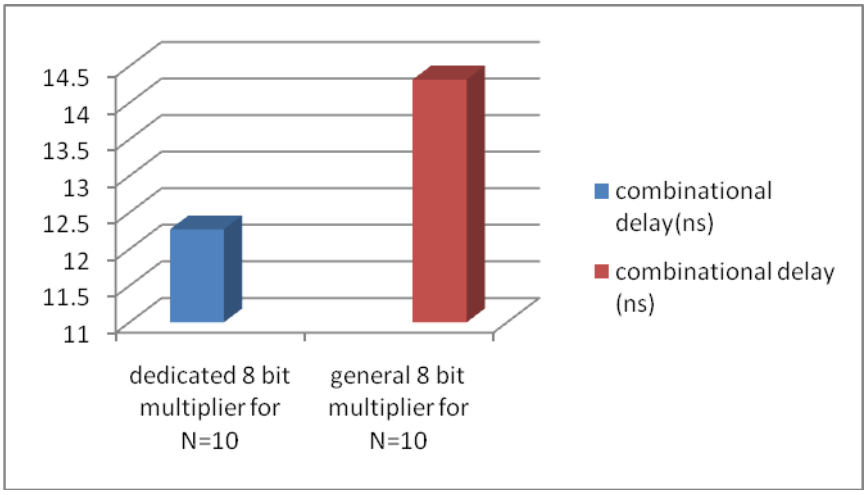


Comparison of modified compressor adder of base paper and purposed one.



Comparison of 8 bit multiplier on basis of with use of multiplexers or not using multiplexers



Comparison of Combinational delay of Dedicated and General 8 bit Multiplier for N=10

V. CONCLUSION AND FUTURE SCOPE

The proposed architecture is based upon 'Urdhava-tiryakbhyam' sutra of Vedic mathematics which is a general multiplication technique for multiplication. This sutra makes the parallel generation of partial products and

removes unwanted multiplication steps. Results shows clearly better improvement of 8 bit multiplier with the use of multiplexers. This proposed optimized Vedic multiplier design may prove to be of great use in future digital signal processing applications, ALU, MAC etc. with stringent demands of speed, area and power. As a future work, the multiplier can be expanded for 16 bits and 32 bits and can be tested for its performance after implementing in an ALU.

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