International Journal of Electrical and Electronics Engineers
Vol. No. 9, Issue No. 01, January-June 2017
ISSN (O) 2321-2055
ISSN (P) 2321-2045

# A LOW POWER CMOS VOLTAGE MODE USING SRAM CELLS

**Sachin Kumar, Uma Shankar**

*Department of Electronics and Communication Engineering, LNCT Bhopal (M.P)(India)*

## ABSTRACT

*In this paper we propose a novel design of a low power static random access memory (SRAM) cell for high-speed operations. The model adopts the voltage mode method for reducing the voltage swing during the write operation switching activity. Dynamic power dissipation increases when the operating frequency of the SRAM cell increases. In the proposed design we use two voltage sources connected with the Bit line and Bit bar line for reducing the voltage swing during the write "0" or write "1" operation. We use 90 nm CMOS technology with 1 volt of power supply. Simulation is done in Microwind 3.1 by using BSim4 model. Dynamic power for different frequencies is calculated. We compare it with conventional 6-T SRAM cell. The simulation results show that the power dissipation is almost constant even the frequency of the proposed SRAM model increases. This justifies the reduction of the dynamic power dissipation for high frequency CMOS VLSI design.*

***Keywords-Low Power, CMOS Voltage, SRAM Cell, DRAM Cell, Frequency***

## I. INTRODUCTION

SRAM is a device that is a key part of the core of a lot of hard ware systems. SRAM stands for Static Random Access Memory. This application note is intended to provide a first time reader an introduction to SRAM basics and structure in SRAMs. SRAM and DRAM are Random Access Memories that can store data as long as power is applied to the device. If the power is removed, all the data that was stored in the memory will be lost; DRAM data could be lost if it is not periodically refreshed, while in SRAMs data can be stored without refreshing, and SRAMs data will remain in the SRAM once it has been written there, and as long as the power supply to the device is maintained; Fig. 1 below shows SRAM Basic Architecture.

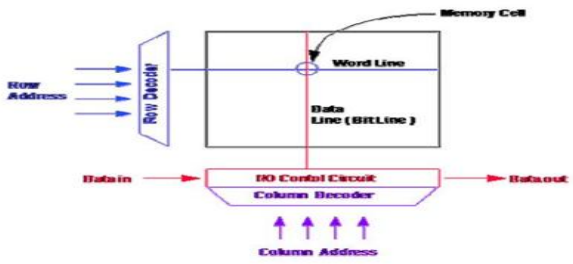


**Figure 1: Basic SRAM architecture**

SRAMs are differentiated from its memory counterparts by the type of the memory cell. Most SRAMs either use a 4-Transistor or a 6- Transistor Memory cell. These cell structures allow data to be stored for an indefinite amount of time in the device as long as powered. Fig. 2 below shows the Memory Cell History the 4 transistor and the 6 transistor cell, 1 transistor cell for DRAM. Cross-coupled inverters form the SRAM cell; Hard- ware system

International Journal of Electrical and Electronics Engineers
Vol. No. 9, Issue No. 01, January-June 2017
ISSN (O) 2321-2055
ISSN (P) 2321-2045

evolution overtime has led to the creation of different types of SRAMs (these referred to as the 4- T and 6- T cells, respectively.)

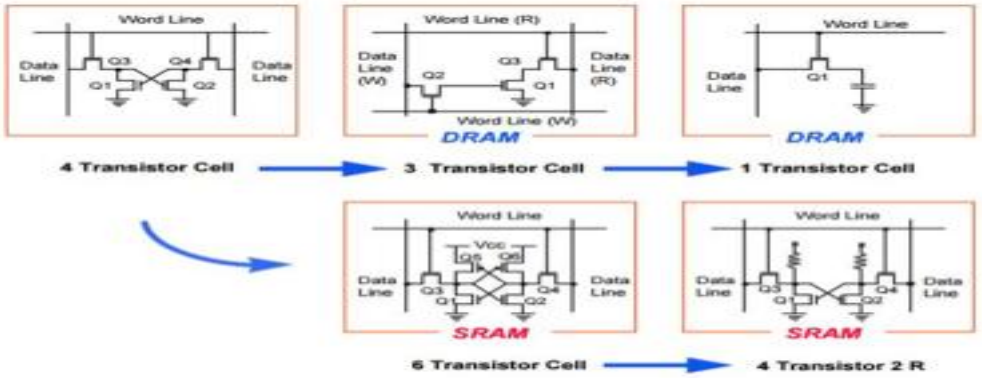


**Figure 2: Memory cell history**

## II. LITERATURE REVIEW

SRAMs basically come in two different flavors: synchronous and asynchronous. Synchronous SRAMs are devices that are synchronized with an external signal clock.

**A. P. Chandrakasan et al. (1995)** presented a technique for minimizing of power consumption for the digital systems, which includes minimization at each and every level of the design in the CMOS. The minimization includes the technology, which is used for the implementation of the digital circuits, the circuit style and topology, the architecture for implementing the circuits and at the highest levels the algorithms that are being implemented.The very vital technology consideration is the threshold voltage and its control, which allows the reduction of supply voltage without having any significant impact on the logic speed. Even further reduction of supply can be made by the use of an architecture-based voltage scaling strategy, which uses parallelism and pipelining, to tradeoff silicon area and power reduction. Since energy is only consumed when capacitance is being switched, power can be reduced by minimizing this capacitance through operation reduction, choice of number representation, exploitation of signal correlations, resynchronization to minimize glitching, logic design, circuit design, and physical design. The low-power techniques that are presented have been applied to the design of a chipset for a portable multimedia terminal that supports pen input, speech I/O and full-motion video.

**V. Patel et al. (2009)** presented an voltage mode quaternary CMOS circuit design using 90nm technology. Good Characteristics and advantages of multi-valued logic (MVL) electronic systems and circuits are created which is of great interest for its practical implementation. Basic gates such as quaternary inverter, NMAX, NMIN and Quaternary multiplexer are designed and simulated. **Behzad Ebrahimi et al** proposed based on the *Vt*-control of the cross-coupled inverters of the SRAM cell to reduce the leakage power when SRAM is in the idle mode. Using the *Vt*-control method along with the built-in feedback leads to increasing the SNM. The proposed schemes have a higher static noise margin (SNM) and lower standby power consumption. The results show considerable improvements in terms of the standby power as well as the hold and read SNM. This suggests that the *Vt*-control method may be used for realizing low-standby power and robust SRAM.**G. Ming et al. (2005)** describes a low-power write scheme by adopting charge sharing technique. By reducing the bit-lines voltage swing, the bit-lines dynamic power is reduced. The memory cell's static noise margin (SNM) is discussed to prove it is a feasible

International Journal of Electrical and Electronics Engineers
Vol. No. 9, Issue No. 01, January-June 2017
ISSN (O) 2321-2055
ISSN (P) 2321-2045

scheme. Simulations results show compare to conventional SRAM, in write cycle this SRAM saves more than 20% dynamic power.

**K. W. Mei et al. (1998)** describes a half-swing pulse-mode gate family that uses reduced input signal swing without sacrificing performance. These gates are well suited for decreasing the power in SRAM decoders and write circuits by reducing the signal swing on high-capacitance pre-decode lines, write bus lines, and bit lines. Charge recycling between positive and negative half-swing pulses further reduces the power dissipation.

## III. PROPOSED WORK

Memory circuits use more than 50% of chip area in processors and ASICs. With increasing demands of high speed processing need of high capacity buffers and cache is increasing. This brings requirement of low power high performance designs of SRAMs. In present literature different SRAM cell structures including 6T, 7T, 8T, 10T and their variations with symmetric and asymmetric configurations. Power reduction in SRAM cell is a complex task, which involves reduction of power without trading off with SNM and access delay of cell. One of the designs under consideration uses voltage-scaling technique to reduce power consumption of the cell.

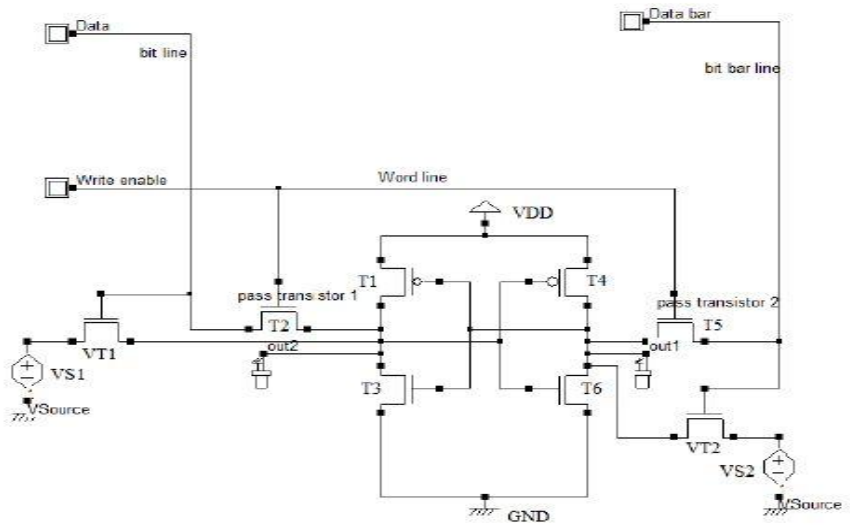


**Figure 3: Proposed design using SRAM**

In the proposed design shown in Fig. 3 above in which we are using two voltage sources VS1 and VS2 connected to the output of the bit and bit bar line. Two NMOS transistor VT1 and VT2 are connected with input of bit and bit bar line directly to switch ON and switch OFF the power source supply during write “0” and write “1” operations, respectively. These power supply sources reduce the voltage swing at the 'out' node when write operation is being performed.

### 3.1 Methodology

- Observe the results of Conventional SRAM cells and other existing SRAM cells.
- Design a Voltage mode method based SRAM cell.
- Compare the results of all conventional SRAM and other existing SRAM cells along with proposed SRAM cell.

International Journal of Electrical and Electronics Engineers
Vol. No. 9, Issue No. 01, January-June 2017
ISSN (O) 2321-2055
ISSN (P) 2321-2045

In order to overcome the drawbacks associated with the conventional 6T SRAM, in this paper, we have modified the classical SRAM configuration. The proposed designed SRAM cell results in almost constant power dissipation even if the frequency increases. In the proposed design we are using two voltage sources VS1 and VS2 connected to the output of the bit and bit bar line. Two NMOS transistor VT1 and VT2 are connected with input of bit and bit bar line directly to switch ON and switch OFF the power source supply during write "0" and write "1" operations, respectively. The proposed design has been illustrated in Figure 3. These power supply sources reduce the voltage swing at the 'out' node when write operation is being performed. A. Write '0' operation During the write '0' operation, bit line is low and bit bar line goes to high. So the transistor VT2 is ON and VT1 goes in the OFF condition. Thus the voltage source VS2 forces to decrease the voltage swing at output of the bit bar line. B. Write '1' operation Similarly when we perform the write '1' operation, transistor VT1 is ON and VT2 goes in to the OFF condition, so the voltage source VS1 decreases the voltage swing at the bit line output. Due to decrease in voltage swing dynamic power dissipation is almost constant even if we increase the frequency of the SRAM cell. So as the frequency increases the dynamic power dissipation also increases because the dynamic power depends upon the operating frequency.

## IV. ANALYSES AND COMPARISON RESULT

In the proposed SRAM model voltage source VSI and VS2 decreases the voltage swing during switching activity. As the frequency increases the switching activity will also be increased but voltage source decreases its voltage swing simultaneously at the output. So at higher frequency the dynamic power dissipation is almost constant.

For proper working of SRAM cell, the size of the transistors is a major factor. The rule of thumb is that the width ratio of the transistor T1 and T2 is nearly equal to 1.5 and the width ratio for T2 and T3 is also equal to 1.5. Similarly it is applicable for transistors T4, T5 and T6, respectively in TABLE 1. This size configuration provides the proper driving voltage to transistors for ON and OFF condition. And TABLE 2 represents the comparison Of Power Dissipation Between The Proposed Vs. Conventional SRAM Cel

**Table I. Width And Length Used In The Proposed Model For Simulation**

| Transistor | Width (nm) |
|---|---|
| T1 | 75 |
| T2 | 115 |
| T3 | 175 |
| T4 | 75 |
| T5 | 115 |
| T6 | 175 |
| VT1 | 300 |
| VT2 | 300 |

**Table 2. Comparison Of Power Dissipation Between The Proposed Vs. Conventional SRAM Cell**

| Operating Frequency | Power Dissipation in 6T SRAM (micro Watt) | Power Dissipation in Propos SRAM cell (micro Watt) |
|---|---|---|
| 500 MHz | 4.890 | 4.977 |
| 1GHz | 8.002 | 5.250 |
| 2GHz | 11.979 | 6.281 |

## V. CONCLUSION

In this paper we propose a novel design for low power SRAM cell by using voltage mode approach. This proposed SRAM cell has two voltage sources, which are used for reducing voltage swing during switching activities. The reduction in voltage swings result in dynamic power dissipation. Dynamic power is for SRAM cell is almost constant for high-speed operations**.**

## REFERENCES

[1] Prashant Upadhyay and R. Kar, D. Mandal, S. P. Ghoshal"A Low Power CMOS Voltage Mode SRAM Cell for High Speed VLSI Design," 2012 Asia Pacific Conference on Postgraduate Research in Microelectronics & Electronics.

[2] A. P. Chandrakasan and R. W. Broderson, "Minimizing power consumption in digital CMOS circuits," Proc. of the IEEE, vol. 83,no.4, pp. 498-523, April 1995.

[3] P. K. S. Vasundara, and K. S. Gurumurthy, "Quaternary CMOS Combiniational Logic Circuits," IEEE Internatinal Conference on Information and Multimedia Technology, pp. 538-542,Dec. 2009.

[4] B. Ebrahimi, S. Zeinolabedinzadeh, and A. A. Kusha, "Low Standby Power and Robust FinFET Based SRAM Design", IEEE Computer Society Annual Symposium on VLSI, pp. 185-190, Jan 2008.

[5] Gu Ming, Yang Jun, Xue Jun, "Low power SRAM design using charge sharing technique," 6th International Conference On ASIC, ASICON, pp.19-23, Oct.2005.

[6] K.W. Mai, T. Mori, B. S. Amrutur, R. Ho, B. Wilburn, M. A. Horowitz, I. Fukushi, T. Izawa, and S. Mitarai, "Low power SRAM design using half-swing pulse mode techniques", IEEE J. Solid-State Circuits, Vol. 33,no.1, pp. 1659-71, Jan. 1998.

[7] A. Karandikar; K. K. Parhi, "Low power SRAM design using hierarchical divided bit-line approach," International Conference on Computer Design: VLSI in Computers and Processors, ICCD '98, pp.82-88, 5-7 Oct 1998.

[8] I. Thoidis, D. Sourdris, I. Karafyllidis, A. Thanailakis, and T. Stoursitis, "Design Methodology of Multiple-Valued Logic Voltage-Mode Storage Circuits", IEEE Internatinal Symposium on Circuit and System, pp. 125-128, March 1998.

[9] R. C. G. da Silva, H. Boudinov, L. Carro, "A Novel Voltage-Mode CMOS Quaternary Logic Design", IEEE Transaction on Electron Devices, vol. 53, no. 6, pp. 1480-1483, June 2006.

[10] Keivan Navi, Roshanak Zabihi, Majid Haghparast, Touraj Nikobin, "A Novel Mixed Mode Current and Dynamic Voltage Full adder", World Applied Sciences Journal, Vol.4,no.2, pp. 289 -294, 2008.

[11] A. Ghorbannia Delavar, K. Navi and O. Hashemipour, "Very Fast Current Mode Logic Gates," CSIT Conference, Yerevan, Armenia, pp. 19-23, June 2005.

[12] Neil H. E. Weste, David Harris, Ayan Banerjee, "CMOS VLSI Design", Pearson Education, 3rd Edition, pp. 55-57.

[13] Islam A, Hasan Mohd. Variability aware low leakage reliable SRAM cell design technique. J Microelectr Reliab 2012; 52:1247–52 [No. 6].