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A PIONEER APPROACH TO MITIGATE LEAKAGE POWER IN CMOS CIRCUIT

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ABSTRACT

In this fast growing age of semiconductor technology, the research field has been entered in nano-scaled or ultrathin regime. Various microcontroller based digital devices are required efficient switching speed, better noise immunity and minimum power delay product. Here, in this paper first reviewed the leakage power of various gates with different designs and highlights their merits and short come. In this work various parameters on established and proposed techniques of various gates are calculated and for verification and validation of this technique, it is implemented on 1-Bit , 2-Bit and 4-Bit full adder circuits. From simulation results proposed circuit saved dynamic power, static power, delay and PDP than other existing techniques. The Adder circuit is implemented by conventional and proposed NAND gate circuit. All simulation is performed by HSPICE simulator by using 32nm Berkley Predictive Technology Module (BPTM).

Keywords: Deep Sub Micron (DSM), Lector Footer Sleep (LFS), Lector Header Sleep (LHS), Lector Header Footer Sleep (LHFS), NAND gate (NG).

I. INTRODUCTION

The urge of high performance and dynamic functionalities in an integrated circuit has led to aggressive technology scaling over the years. In Deep Sub-Micron (DSM) technology, more number of gates are to be integrated on a single chip, so as to result in small geometries. But with this power densities and total power are rapidly increasing. Design of low power circuits has become important in a variety of application. However reducing power consumption involves a trade-off between timing and area at different stages of the design. The successful power sensitive design requires engineers to accurately and efficiently be able to perform these trade-offs. To handle these issues efficiently, it is essential to understand the different types and source of power dissipation in the digital complementary metal oxide semiconductor (CMOS) circuits. The reason for choosing the CMOS technology is that it is the most dominant digital IC implementation technology. This chapter defines some of the most significant power dissipation sources in CMOS circuits. Then some low power design techniques of handling leakage power are discussed.

II. LITERATURE REVIEW

The main concentration of this research is to find out the low power circuit level technique for digital circuit design. Hence different circuit styles from traditional to non traditional techniques are reviewed. Various research findings merit-demerits of all techniques are discussed.

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***Kaushik Roy et. al.*, 2003,** reviewed all causes of leakage current in transistor that includes gate drain leakage, gate-oxide tunneling, drain-induced barrier lowering and weak inversion effect. They observed that the low threshold voltages, gate leakage and sub-threshold voltages are the dominant sources of leakage current in deep sub-micron meter devices. Effect of such sources will increase with technology scaling. The GIDL and BTBT (base to base tunneling) may also have a significant effect on advanced CMOS devices.

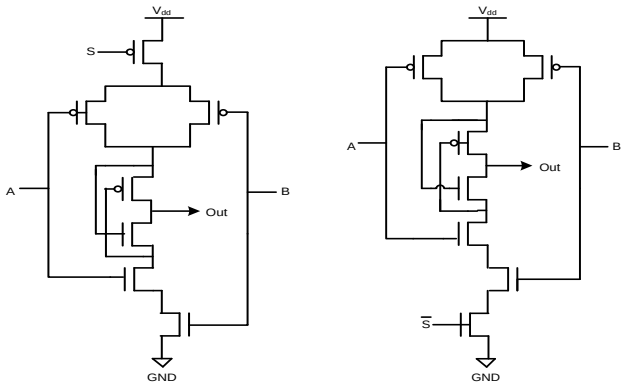
A. Agarwal et.al, 2006, All internal signals are set to logic values to achieve minimum total leakage current in the circuit. Since the leakage current in a CMOS gate is mainly dependent on the combinations of logic values applied to input signals. Hence such method reduces leakage current in CMOS device.

***Jing Yang and Yong-Bin Kim*, 2013**, describes two runtime methods in their research paper to reduce leakage current in CMOS circuits. In both methods it is assumed that the device will produce a 'sleep signal' to indicate the circuit is in standby mode. In first method, pre-selected internal signals and a new set of external inputs are shifted by 'sleep' signal into the circuits.

***Zia Abbas and Mauro Olivieri*, 2014,** this paper presented a detailed study of leakage current mechanisms in CMOS image sensors. They investigated reverse current–voltage characteristics of sensors at 0.045 µm CMOS technology. They conclude that in p-n junction of MOS transistor, tunneling and ionization impact are the dominant mechanisms for leakage current.

III. PROPOSED WORK

In this section of paper some innovative techniques are introduced namely LECTOR Header Sleep (LHS), LECTOR Footer Sleep (LFS) and LECTOR Header Footer Sleep (LHFS), these are the combinations of self controlling and external leakage controlling technique. In self controlling technique no external signals are applied while in external leakage controlling technique external sleep signal are applied which switches OFF the sleep transistor to reduces the leakage power. The basic idea behind all the proposed techniques is to provide stacking effect of the transistor which mitigates leakage power from supply voltage to ground. Proposed LHS, LFS and LHFS approaches are implemented for two input NAND gate as shown in Fig. 1. (a), (b) and (c). Proposed circuit reduces the leakage power by providing stacking effect with LECTOR technique and inserting of sleep transistor over pull up and pulls down network which rail from V_{dd} to GND and increase the resistance of the circuit which helps in to mitigate the leakage power when circuit is in idle mode.



(a) LHS (b) LFS

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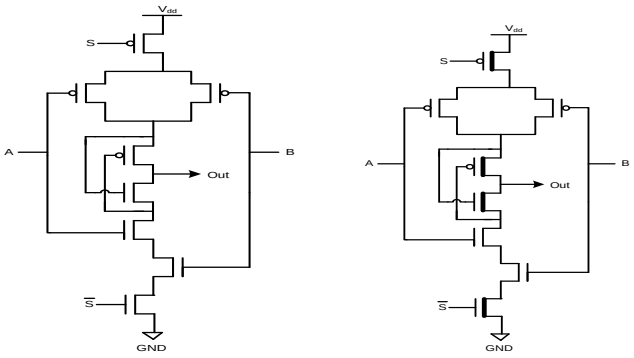

(c) LHFS with low Vth (d) LHFS with High Vth

Fig.1: Proposed Leakage reduction techniques

For verification and validation Lector Header Footer Sleep technique is implemented on 1-Bit , 2-Bit and 4-Bit full adder circuits.

One Bit FULL ADDER Circuit (1 Bit FA)

One Bit Full Adder circuit implemented by nine NAND gate which outputs gives SUM and Carry signal respectively.Each NAND gate exhibits the LHFS. The circuit of 1-Bit FA is shown in Fig.2.

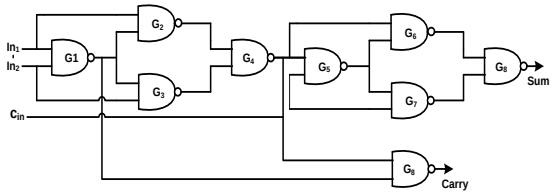

Fig.2. One Bit FULL ADDER (1 Bit FA) Circuit

Two Bit FULL ADDER Circuit (2 Bit FA):

Two, one bit full Adder with LHFS is connected in parallel to give 2-Bit FA circuit, which shown in Figure 3.

(i) Circuit Diagram

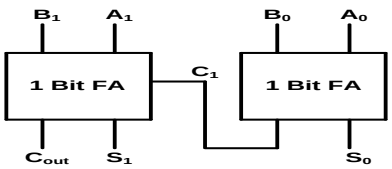

Fig.3: Two Bit FULL ADDER (2 Bit FA) Circuit

Four Bit FULL ADDER Circuit (4 Bit FA) :

Figure 4 , depicts 4-Bit Full Adder with LHFS circuit, implemented by four parallel connection of one bit Adder with LHFS circuit.

(i) Circuit Diagram

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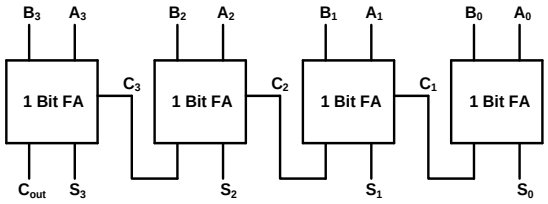

Fig.4: Four Bit Full Adder Circuit

The output wave form of basic, existing and proposed circuit for two inputs NAND gate is shown in Fig.5, here it can be seen that the LECTOR and proposed circuits does not achieve proper logic level because location of leakage controlled transistors is such a way that there is a small degradation of output voltage.

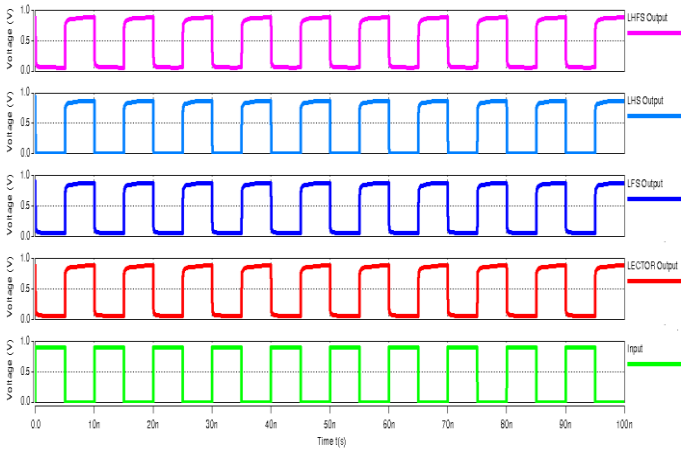

Fig.5: Transient characteristics waveform of 2-input proposed NAND gate

V. RESULT AND DISCUSSION

In this section the power dissipation of existing and proposed leakage reduction techniques is calculated. All the warmed- over and proposed technique are simulated in HSPICE at 32nm technology with supply voltage of 0.9V, output capacitance C_L =1pF, Leakage power is investigate at different temperature, The size (W/L) of all existing and proposed circuit made from P-MOS and N-MOS is same for fair comparison of results.

Table. I. Average Power Consumption at 32nm Technology

Techniques	Dynamic Power (µW)		Delay (ps)		PDP (aWS)	
	Low Vth	High Vth	Low Vth	High Vth	Low Vth	High Vth
NG	0.1324	0.0854	6.815	11.11	0.902	0.948
NGHS	0.1486	0.0983	10.56	17.18	1.562	1.688
NGFS	0.1251	0.0845	9.398	16.05	1.175	1.356
NGHFS	0.1477	0.1024	13.40	22.82	1.197	2.336
LECTOR	0.1131	0.0818	9.353	25.86	1.057	2.115
LHS	0.1256	0.0894	14.28	35.27	1.793	3.153
LFS	0.1145	0.0815	7.387	33.24	0.845	2.709
LHFS	0.1163	0.0720	16.89	41.12	1.216	2.960

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A pioneering LHS, LFS and LHFS leakage reduction technique is proposed for low power application in digital circuits. Results show 32nm technology is used for low power applications, reduction is to design a device which is having lowest possible leakage. The experiment results shows that saving of dynamic power in proposed LHFS circuit is much lower than other circuits, the reduction is about 17.17% in NG, 25.68% in NGHS, 12.85% in NGFS, 25.75% in NGHFS and 2.86% in LECTOR. The proposed technique can be applied on high performance, low power applications, where leakage is a main concern.

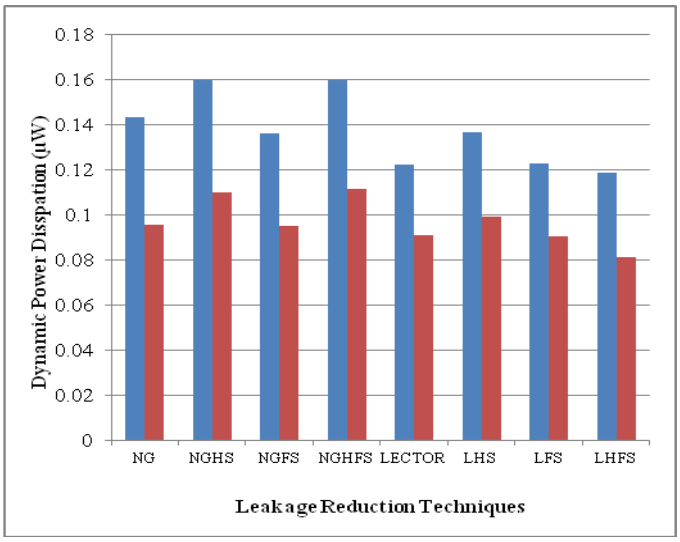

Fig.6. Dynamic Power Dissipation of existing and proposed technique

The result shows comparison between basic gate design and proposed hybrid gate approach. It has been clearly shown in the bar graph; the leakage power consumption is more in basic design circuit as compared to our proposed hybrid gate technique as shown in Fig.6

Table.II. Conventional Adder Circuit Design by Using LECTOR Technique

Sr.	Adder Circuit	Power Dissipation			Delay (ps)	PDP(E-18j)	
		P_D (uW)	P_{ST} (nW)	$P_{T\,(uW)} = P_D + P_{ST}$		PDP_D	PDP_{ST}
1	1-Bit	0.65	54.40	0.70	14.6	9.49	0.7942
2	2-Bit	0.63	16.50	0.65	14.7	9.261	0.2425
3	4-Bit	0.52	4.90	0.52	16.2	8.424	0.0793

Simulation result of 1-Bit, 2-Bit and 4-Bit Full Adder circuit designed by using LECTOR Technique is shown in Table II. The parameters such as dynamic power ($P_{D)}$, static power ($P_{ST)}$, total dissipated power ($P_{T)}$, delay and Power Delay Product (PDP) are calculated and tabulated.

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Table .III. Adder Circuit Design by Using Proposed (LHFS) Technique

Sr.	Adder Circuit	Power Dissipation			Delay (ps)	PDP(E-18j)	
		P_D (uW)	P_{ST} (nW)	$P_{T\,(uW)}$ $=P_D+P_{ST}$		PDP_D	PDP_{ST}
1	1-Bit	0.48	37.44	0.52	16.87	8.0976	0.6316
3	2-Bit	0.47	15.90	0.49	16.2	7.614	0.2575
4	4-Bit	0.42	4.33	0.42	18.9	7.938	0.0818

Simulation results of 1-Bit, 2-Bit and 4-Bit Full Adder circuit designed by using proposed LHFS Technique is shown in Table III. The parameters such as dynamic power ($P_{D)}$, static power ($P_{ST)}$, total dissipated power ($P_{T)}$, delay and Power Delay Product (PDP) are calculated and tabulated in table III.

V. CONCLUSION

The research focused on mitigating the leakage power, improving switching delay and power delay product in next generation DSM technology. It reflects upon dominating face of leakage power dissipation in DSM VLSI design during idle mode. The experiment results shows that saving of dynamic power in proposed Lector Header Footer Sleep circuit is much lower than other circuits, the reduction is about 17.17% in NAND Gate , 25.68% in NAND Gate Header Sleep , 12.85% in NAND Gate Footer Sleep , 25.75% in NAND Gate Header Footer Sleep and 2.86% in LECTOR. The result of 1-bit, 2-bit and 4-bit Full Adder circuits designed by proposed technique is also much improved compare to the conventional Lector technique. Therefore proposed techniques can be applied on high performance low power applications.

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