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A REVIEW ON PIPE LINE ANALOG TO DIGITAL CONVERTER USING 0.18µm CMOS TECHNOLOGY

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ABSTRACT

This paper describes a 12-bit pipeline ADC (Analog-to-Digital Converter) for CMOS (Complementary Metal Oxide Semiconductor) that is implemented in a TSMC 0.18µm CMOS process. The proposed ADC utilizes the Threshold Inverter Quantization (TIQ) technique that uses two cascaded CMOS inverters as a comparator. The TIQ flash ADC achieves high speed, small size, low power consumption, and low voltage operation compared to other ADCs the sample and hold circuit have high Sampling rate. This Design is implemented and Fabricated in TSMC 0.18µm CMOS verified on the LT SPICE in 0.18µm Technology.

Keywords : Pipe line ADC, CMOS transistor

I. INTRODUCTION

The minimum channel length of the transistor will be scaled down to 0.065 µm in 2007 according to the roadmap of semiconductors [13]. In addition to this downscaling, today's system-on-chip (SoC) trend forces analog and mixed-signal integratedcircuits (ICs) to be integrated with complex digital processors and memory on a single.

Chip-called complete SoC or digital and mixed-signal (D/MS) SoC. At present, there are many demands on the complete SoC in wireless and broadband communications wireless networking (WLAN, voice/data communication, and Bluetooth), wired communication (WAN and LAN), and consumer electronics (DVD, MP3, digital cameras, video games, and so on). Therefore, as one of the mixed-signal ICs, analog-to-digital Converters (ADCs).

Have to follow this complete SoC trends. This chapter introduces the challenges in designing ADCs and possible solid-state technologies for the complete SoC trends. The pipelined ADC can operate at a high speed, but it is slower than the flash. It covers sufficient range of applications due to its flexible resolution and speed[1].

1.1 Pipelined ADC:

The pipelined ADC architecture is a type of sub-ranging ADC introduced in the previous section. This architecture is implemented with at least two or more low-resolution flash ADCs as shown in Fig. 1. Each stage has a S/H circuit to hold the amplified residue from the previous stage. Further input is applied to low resolution flash ADC to generate a segmented binary output. Like the sub-ranging ADC, thsegmented output is changed to an analog s/g and subtracted from the i/p. Thisresidue is amplified in an amplifier to send to the next stage. The segmented binary outputs from each stage are time-aligned with a shift register. The final binary output

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is obtained after passing through digital error correction logic. This conversion process in the pipelined ADC is shown in Figure 1.[5]

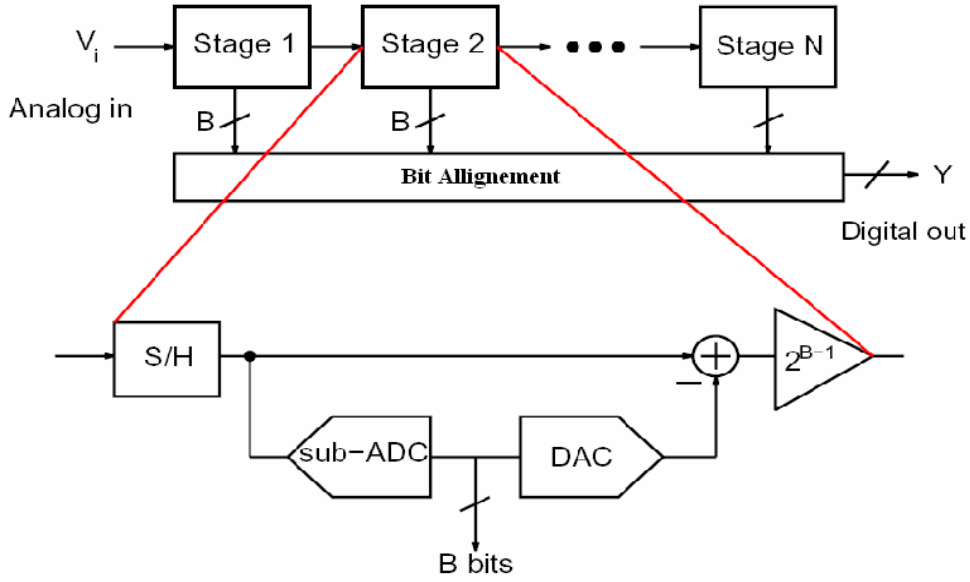

Figure.1BlockdiagramofapipelinedADC

1.1 Operation Of Pipeline Adc

Each stage takes its input, multiplies it by 2, and adds of subtracts the reference voltage depending on the bit of the previous output. This is mathematically described as[7].

$$Vi = 2* Vi_{-1} - bi_{-1} * V_{ref}$$

$$bi = \begin{cases} +1 \text{ if } Vi\text{-}1 > 0 \\ -1 \text{ if } Vi\text{-}1 < 0 \end{cases}$$

II. PROPOSED METHOD

Pipeline architectures transfer the residual from one stage to another. An amplification factor relaxes the accuracy requirements of the successive stage. The limit to accuracy for conventional pipelines comes from the ADC, the DAC and the analog blocks used to generate the residual The aim of the project is to design a 12-bit pipeline ADC Design parameters include input range, conversion speed, resolution, power consumption, physical dimensions, etc. This design is not targeted to one special application, so the design specifications are not strictly following any application standard. The general guideline is to design a high speed, low power pipeline ADC with wide input bandwidth. Each block of project is designed at transistor level and design is simulated on LT Spice Swicher CAD –III schematic editors simulation tool, schematic editor (is used for design entry. TheSimulator after simulation provides respective waveforms. The design is implemented on TSMC018 technology with feature size of 0.18 micron [10].

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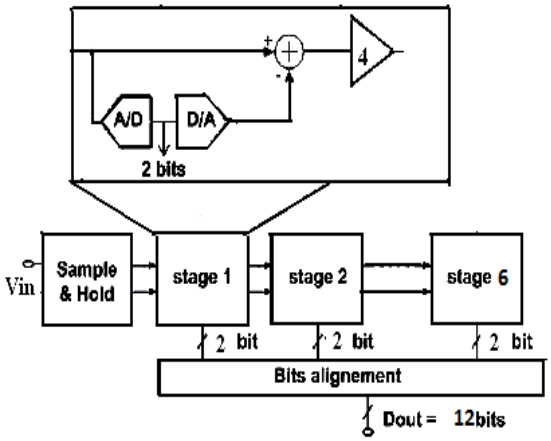

Figure 2 Block diagram of proposed pipeline ADC

2.1 Design Specifications

- Resolution = 12-bit
- Supply Voltage Range =-1.8 V to + 1.8 V
- Analog Input Voltage Range = ± 1V
- Maximum Input frequency >50MHz
- Maximum Sampling rate >40 MHz
- Sample and Hold stage. DC Gain= 1 V/V
- Power Dissipation = ≥ 25mw
- Technology of design : TSMC 0.18 µm

III. LITERATURE SURVEY

Literature survey based on some recent development of pipe line ADC various methods are studied with their conclusion and methodology.

J. Bouvier et.al The design of a full integrated electronics readout for the next ILC ECAL presents many challenges. Low power dissipation is required, and it will be necessary to integrate together the very front-end stages with the analog to digital converter. We present here a 12 bits 25 MHz analog to digital converter using the pipe line architecture. Its' first stage is a charge redistribution sample and hold, then follow ten 1.5 bit sub-ADC and finally a 2 bit flash. A CMOS 0.35 mu process is used, and the dynamic range covered is 2V. The analog part of the converter can be quickly switched (a couple of mus) to a standby mode that reduces the DC power dissipation by a ratio of 1/1000. The size of the converter's layout including the digital correction stage is only 1.7 mm * 0.6 mm, and the total dc power dissipation is 35 mW.

Ramin Zanbaghi et.alA fully integrated CMOS base-band part of a low-IF WPAN receiver is presented, which consists of an active complex filter, an automatic gain control unit, and a 10-Bit Pipe-Line ADC. The highlights of the receiver include a low- power active complex filter with a nonconventional Gm-C structure and a high-resolution, low power pipe line ADC using averaging and double sampling techniques. The chip was designed

on a small die using 0.18-um standard CMOS process. The filter provides more than 55 db image rejection ratio and IM3 of -50 dB for 1.9 & 2.1 MHz signals with 0.2Vpp. The converter has a peak SFDR of 61 dB, maximum DNL of 0.5 LSB, and INL of 0.9 LSB. The all parts of the scheme consume an active current about 4mA from a 1.8-V power supply.**Vineet Sharma et.al** This paper proposes a fully digital sensor interface. For this, an analog to digital converter (ADC) and time to digital converter (TDC) based on a common time based ADC (TAD) architecture has been investigated.

It is concluded that the proposed fully digital time-based ADC architecture can also be operated as TDC. The fully digital circuit has a ring delay line (RDL), latch, encoder and a synchronous counter. The circuit is implemented in 0.18µm digital CMOS, achieving 139µV/LSB (14-bit, 1-MS/s, 1.6 mW) in ADC mode and 227 ps/LSB (V_{IN} = 1.0 V, 14-bit), 94 ps/LSB (V_{IN} = 1.8 V, 14-bit) in TDC mode respectively. In addition to the scalable design, the resolution of both TDC as well as ADC, can be set by a variable input voltage, V_{IN}.

Teng-Chieh Huang et.al in this paper, an area-power-efficient 11-bit hybrid analog-to-digital converter (ADC) with delay-line enhanced tuning for neural sensing applications is presented. To reduce the total amount of capacitance, this hybrid ADC is composed of a coarse tune and a fine tune by 3-bit delay-lined-based ADC and 8-bit successive approximation register (SAR) ADC, respectively. The delay-lined-based ADC is designed to detect the three most significant bits by a modified vernier structure. To relax the accuracy requirement of the coarse tune, the lifting-based searching algorithm and re-comparison procedure are proposed for the fine tune. To further achieve energy saving, split capacitor array and self-timed control are utilized in the SAR ADC. Fabricated in TSMC 0.18µm CMOS technology, an ENOB of 10.4-bit at 8KS/s can be achieved with only 0.6µW power consumption and 0.032-mm^2 area. The FoM of this ADC is 49.4fJ/conversion-step.

Yan Li Hang et.al Avoiding use of traditional high-speed analog-to digital converters (ADCs) and constant fraction discriminators, Multi-voltage threshold (MVT) method is able to digitally sample positron emission tomography (PET) scintillation pulse with reasonable cost. As the key component of the MVT method, a time-to-digital convertor (TDC) with high resolution

And large dynamic range is presented in this work. The TDC architecture uses a delay locked loop (DLL) to generate the fast clock edges from a 100 MHz clock, and a 32-stage Vernier delay lines (VDL) is used to achieve the 40pS timing resolution. The proposed TDC is designed using the standard 0.25 µm CMOS technology with 2.5V normal supply voltage. The power consumption of the TDC is ~70 mW.

IV. CONCLUSION

The Design and implementation of 12-bit pipeline ADC is to be design on TSMC 0.18µm technology. The design is implemented in LT Spice Schematic Editor and the results will be verified with CAD-III. Total power dissipation will be less than 12 mw, resolution 12 bit. The TIQ flash ADC achieves high speed, small size, low power consumption, and low voltage operation compared to other ADCs.

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