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ESTIMATION OF AREA, POWER AND DELAY OF DIFFERENT IOs-VECTOR LENGTH KOGGE STONE ADDER

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ABSTRACT

An Adder is a fundamental block for an arithmetic operation and is the base of other mathematical operations like subtraction, multiplication and division. Kogge Stone Adder is analogous to both Parallel Prefix Adder (PPA) and Carry Look Ahead (CLA). In this paper, basic form of Kogge Stone Adder is analysed to expand the circuit for bigger calculations for future purpose. On the basis of studies self comparisons are made between different bit sizes of Kogge Stone Adder on the basis of delay, area and wiring congestion.

Keywords: ***Adder, Parallel Adder, Propagated Carry, Generated Carry, Delay.***

I INTRODUCTION

Addition is a vitally necessary operation in any Digital, Analog, or Control system. Fast and precise operation of digital system depends on the capabilities of adders. The function of adder is to fasten the addition of partial products generated during the multiplication operations. Kogge Stone Adder uses different adders combined for its functioning like tree adders, Parallel Adders and Carry Look Ahead Adders.

In tree adders, carries are generated in parallel and fast computations are obtained due to increased area and power. The main advantage of the design is that the carry tree reduces the number of logic levels (N) by essentially generating the carries in parallel. Whereas, the parallel-prefix adders are more favourable in terms of speed due to the complexity i.e. log2 N delay through the carry path as compared to that of other adders.

Kogge-stone adder is the fastest adder when compared to other adders. The adder priority in terms of worst-case delay is found to be Carry-Look-Ahead and Kogge-Stone. This is due to the number of "Reduced Number of stages". Implementation of Kogge-Stone adder is straightforward while comparing with others, and also it has one of the shortest critical paths of all tree adders. But while comparing among different bit sizes, the drawback with the Kogge-Stone adder implementation is the large area consumption in higher bit size computations.**[1]**

Basic Principle of working includes production of Generated Carries in last stage and generated carries XORed with initial propagated carry used to produce Summation bits.

A carry-look ahead adder speeds up by reduction in the amount of time required to determine the carry bits. It can be compared with the simpler adder, for which the carry bit and sum bits are calculated simultaneously, and each next bit must wait until the previous carry has to be calculated to begin calculating its own result and carry

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bits. The carry-look ahead adder computes one or more carry bits before the summation bits, which results into reduction of the wait time to compute the result of the larger value bits.

A Parallel Prefix Adder (PPA) works in three main stages and could be named as the Pre-processing stage, Carry Graph stage and Post-processing stage.

The pre-processing part will lead to the generation of the propagate (p) and generate (g) bits. The acquirement of the PPA carry bit differentiates it from other type of adders. It uses a parallel form of computing the carry bit that makes it performing addition arithmetic faster.**[2]** The proposed Parallel Prefix adder for 64-bits has been proposed. **[3]**

II STAGES FOR GENERATION OF CARRY

2.1. Stage 0

In this stage, Input signals are used to generate carry i.e. propagated carry and generated carry with the help of Input of each adder. 'x_i' and 'y_i' are the input signals, whereas 'P_i' and 'G_i' are the carry input signals. Here 'i' represents bit position. This stage is referred as Stage-'0'.this stage is also known as pre-processing stage. KGS represent a range of the near-minimum logic depth [2]These signals can be calculated by following equations (1) & (2)-

$P_i = x_i$ XOR y_i …… (1)

$G_i = x_i$ AND y_i ……..... (2)

2.2. Stage 1

In this stage, carries corresponds to each bit is computed.stage 1 is named as carry look-a head processing. In this stage carry look a head adder methodology is used to propagate and generate carry. Carry look ahead adder compute the one or more carry before calculating the sum.[3]which reduce time to calculate the sum of large bit size.

Both carry operator contains two AND gates and one OR gate. Operator uses propagate and generate as interconnected signals and given by equations (3) & (4)-

$P_i = P_i$ ANDP_{i-1}……...(3)

$G_i = G_i$ OR (P_i AND G_{i-1}).....(4)

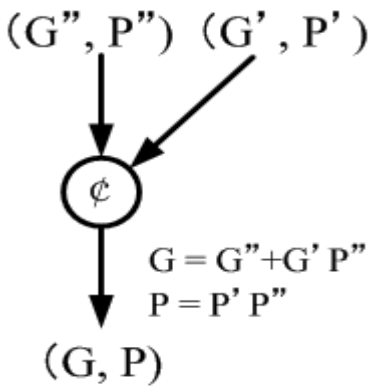

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Fig. 1. Tree Network[4]

Above equations show that carry complexity increase with bit size of the adder. At a time multiple processing takes place in parallel hence Kogge Stone Adder is normally referred as Parallel Prefix Adder. To avoid the delay and complexity introduce Kogge stone adder with the modification of carry look-a head adder. Equation (3),(4) calculate propagate and generate carry up to N^{th} bit width.

2.2.1 Bit Size and Stage

Bit size and stages has mathematical relation in Kogge stone adder .

$N=2^n$ ……(1)

Here N= bit size; n= number of stages;

Bit size	Number of stages
8	3
16	4
32	5
64	6
128	7

Table. 1. Different Bit Size

2.3. Summation Process

In this final stage to calculate the sum and carryout of the input bits. This stage gives the final output of the adder. Generated carries are treated as final carries in the this stage. The sum bits (S_i) and carry bits (C_i) are given by following equations-

$S_i= P_i$ XOR C_{i-1}…… (7)

$C_i= g_i$ …… (8)

While calculating carries bits, the circuit requires an initial carry i.e. 'C_{in}'. Hence C_{in} is kept '0' initially and therefore the initial carry bit i.e. $C_0= C_{in}$. C_{in} is also used as a carry while executing initial summation bit i.e. 'S_0'. **[7]**

III 4-BIT ADDER

When the width of input bit is 4 then Kogge stone adder computer the sum and carry in two stages. It takes log2N time to generate carry[6].it considered as fastest adder design.

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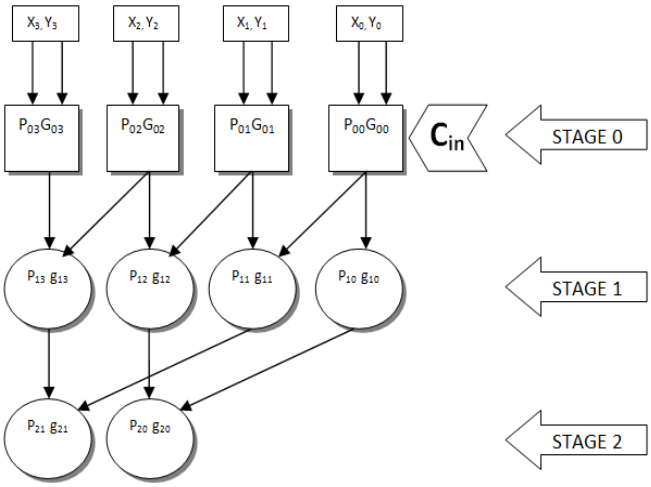

Fig. 2. 4-Bit KSA Adder Network

Above figure shows network and stages for a 4-bit Kogge stone adder (see fig. 2). The functioning of higher bits adders like 16 or 32 bits could be understood from this basic diagram as the equations for various stages remains the same.[4]

Further, explanations can be done by an example illustrating simple 4-bit addition. In fig. 4, two 4-bit binary numbers i.e. '1011' and '1000' are added using a Kogge stone adder. From equations for each stage as stated earlier, the flow diagram could be prepared as of network fig. 3. In stage '0' carry input signals are generated using equation (1) and (2). Thereafter propagated carry and generated carry bits are executed using equation (3), (4), (5) and (6) in stage '1' and '2'. Finally, from a simple adder principle sum bits and carry bits are generated from equation (7) and (8).

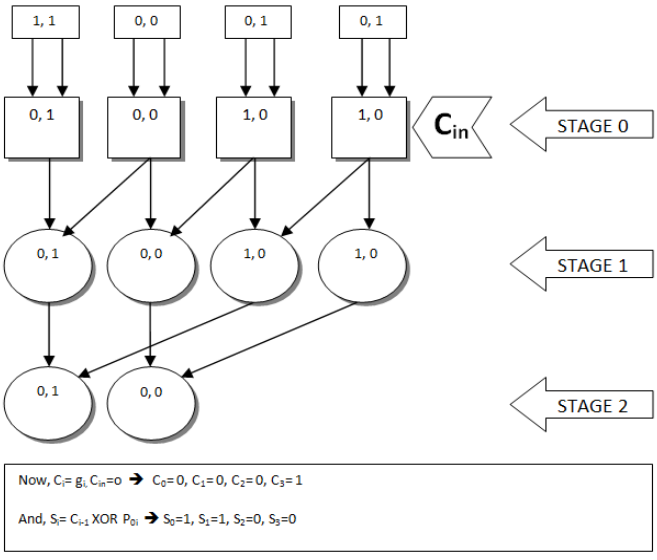

Fig.4. Addition of two 4-bit binary numbers KSA logic

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The main advantage of Kogge stone adder is its mechanism as all the stages are working in parallel. After all the calculations, proper sequencing of bits is done to get proper summation. As shown in fig. 4, after arranging sum bits from S_0 to $S_3$and then 'C_3'i.e. final carry sum is obtained. From fig. 4, the sum of '1011' and '1000' comes out to be '10011'.using Xilinx 14.1 software with the help of VHDL output of 4 bit adder .refer fig.5

Fig.5. Output of Two 4-Bit Binary Numbers KSA Logic

Using Xilinx14.1 FPGAs technique on artix7 RLT view of 4 bit Kogge stone adder. Here clock pulse is enable to '1' in this circuit.

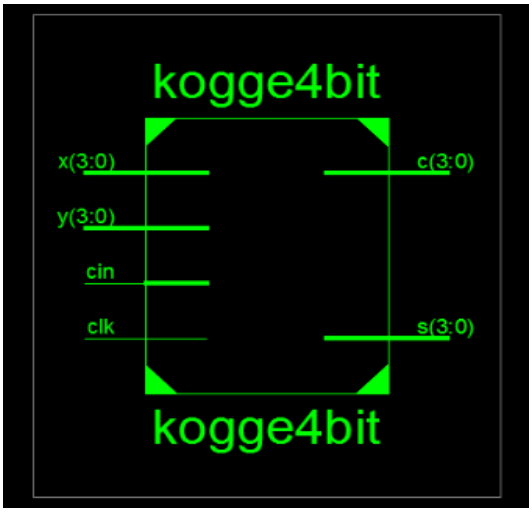

Fig.6. RLT view of 4 bit adder

IV 8-BIT ADDER

IOs vector length is 8.so it has different parameters with 4 bit KGS. KGS 8 bit has 3 stage as shown in fig.7. Quiescent power of 8-bit adder is 99miliwatt.it has 36 slices of LUTs and 34 input and output pins in the

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Vol. No. 9, Issue No. 01, January-June 2017
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network. stage 0 is calculating with the help equation (1)and equation (2).then stage 1 will compute with the help of equation (3) and (4).in each case i-1 will take as previous propagate and generated carry.

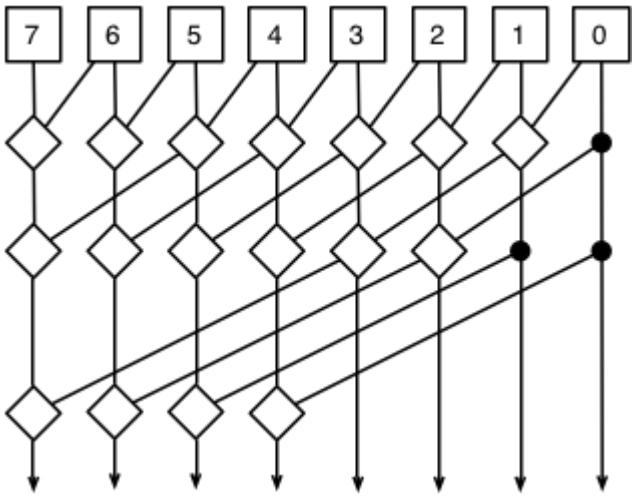

Fig.6. 8-Bit KSA Adder Network

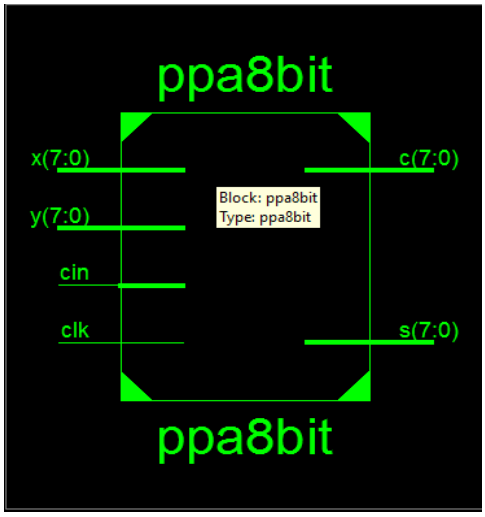

Fig.7. RLT View of 8-Bit Adder

V 16-BIT ADDER

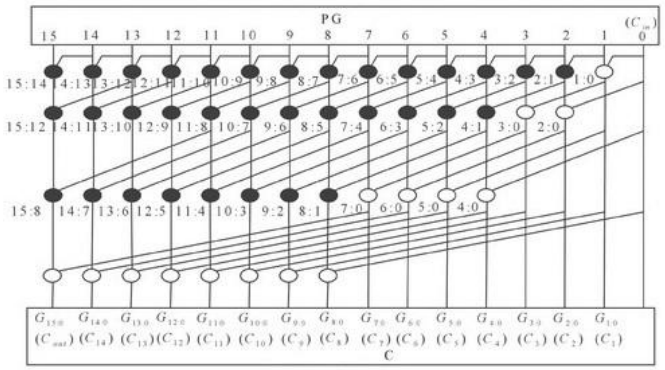

Fig.8. 16-Bit KGA Adder Network

In [11] author considered several Kogge stone adder implement on Xilinx on different FPGAs.KGS is a representative of tree adders.16-bit has 100 slice of LUTs and 66 input and output pin. stage 2 is working on 4 level.

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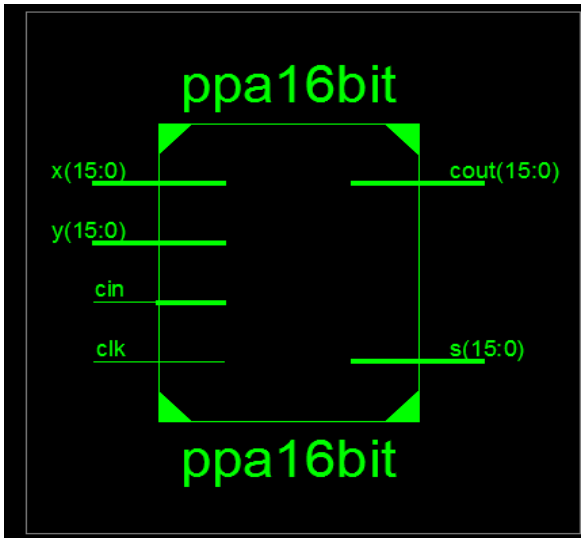

Fig.9. RLT view of 16- bit adder

VI 32-BIT ADDER

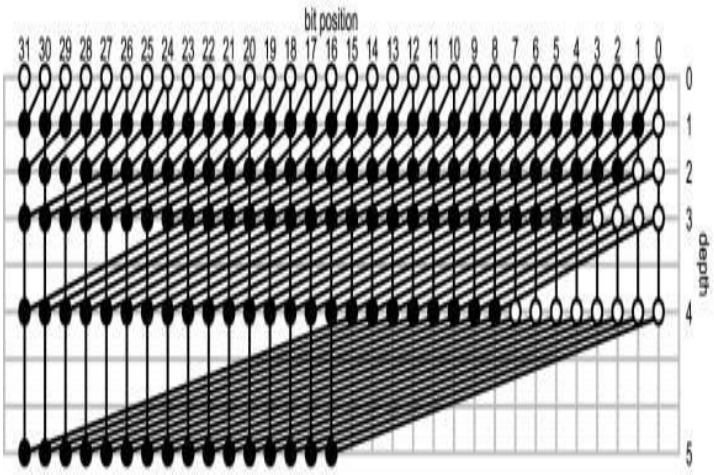

Fig.10. 32-Bit KGA Adder Network

In [13] stage 0 in architecture network of 32 bit prefix adder involves the arrangement of generate and propagate carry signal signal. In 32 bit network stage 1 has internal level and generate carry with the help of equation (3) and (4).32-bit has minimum period 1.932ns with 130 input and output pins.

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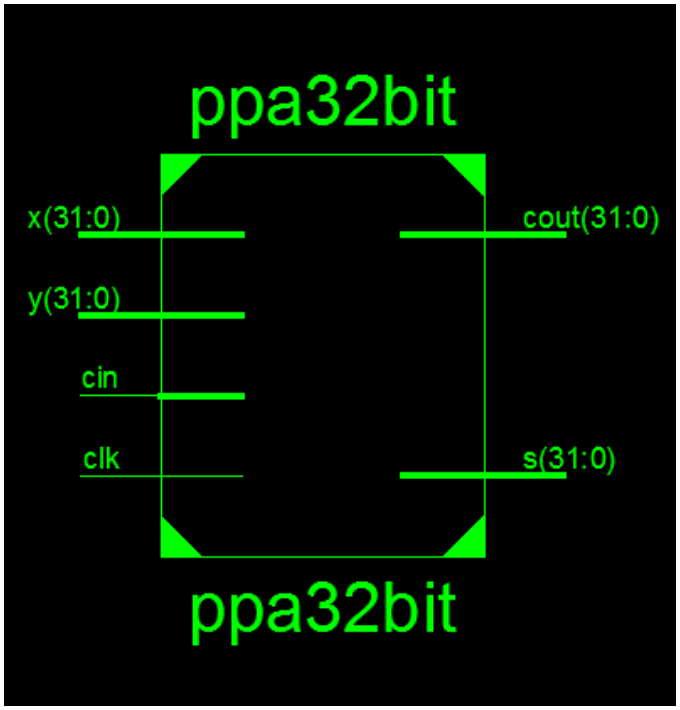

Fig.11. RLT View of 32- Bit Adder

VII 64-BIT ADDER

64-bit adder has 6 level in stage 2. [13] final stage involves band of sum and carry signal.stage 0 is fast because they involve only simple operation signal local to each bit position.64 bit adder has 258 input output pins when it design on Xilinx artix7 on XC7A350T and package FFG1156.

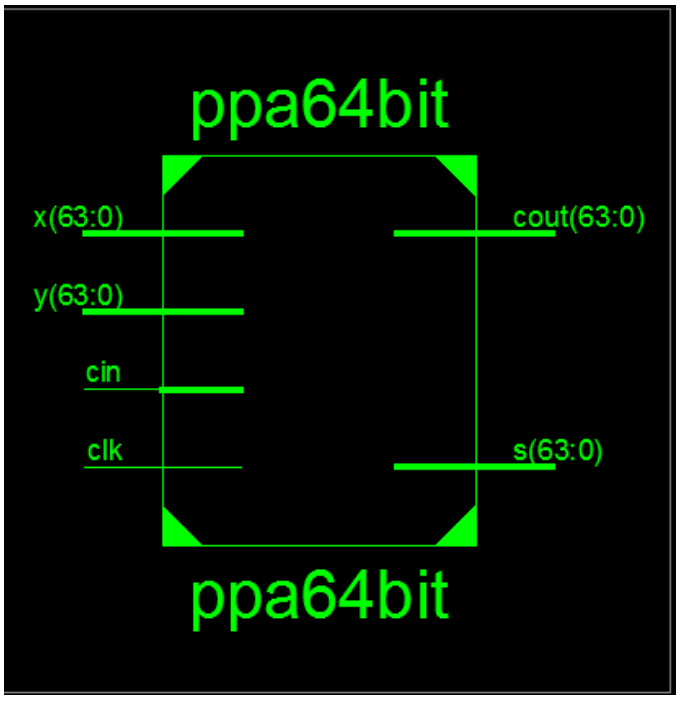

Fig.12. RLT View of 64- Bit Adder

International Journal of Electrical and Electronics Engineers
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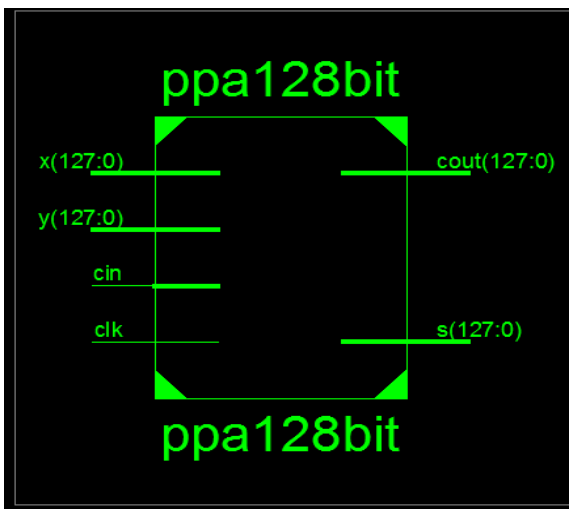
ISSN (O) 2321-2055
ISSN (P) 2321-2045

VIII 128-BIT ADDER

In [12] the delay of Kogge stone adder adder with proposed algorithm is 21.959ns on Xilinx ISE navigator12.3. with Xilinx 14.1 FPGAs artix 7 delay reduce 3.425ns with 514 input and output pins and 1540 LUTs.



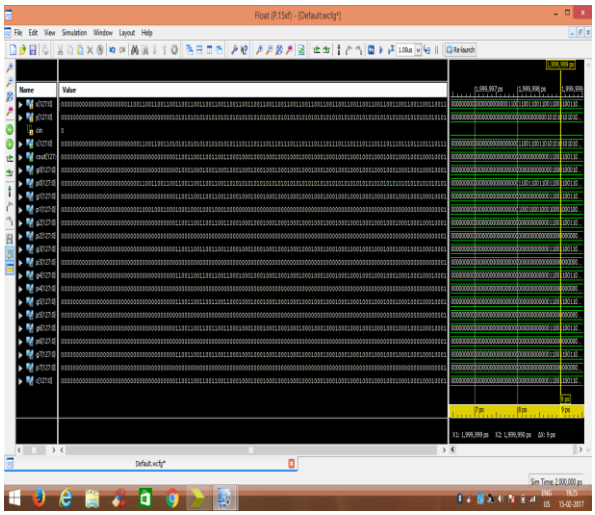


Fig.12. RLT view of 128- bit adder Fig.13. Output of 128- Bit Adder Using Xilinx

IX RESULTS

In term of delay power and area of Kogge stone adder with different IOs vector length.

	100 MHz	250MHz	500MHz
8-bit	55	131	167
16 –bit	127	172	247
32-bit	153	238	388
64-bit	227	407	728
128-bit	355	743	1036

Table.1.Analysis of Power Distribution

In table.1 analyze the power on different frequency. And find the static power of the circuit. Dynamic power in each case appox .098 watt. The above power unit is miliwatt.

	Minimum time	Maximum frequency

International Journal of Electrical and Electronics Engineers
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ISSN (O) 2321-2055
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8-bit	1.592ns	628.14MHz
16-bit	1.91ns	522.738 MHz
32-bit	1.932ns	517.598 MHz
64-bit	2.88ns	346.741 MHz
128-bit	3.425ns	291.97 MHz

Table.2.Critical Time Analysis

	Number of slice LUTs	Number of occupied slices	Number of bonded IOBs
8-bit	36	16	34
16-bit	100	95	66
32-bit	197	95	66
64-bit	644	429	258
128-bit	1540	998	514

Table.3.Area Parameters

According to [12] 128-bit Kogge stone adder has delay of 21.956ns. According to [7] delay of 16 and 31- bit Kogge stone adder is 12.84 and 11.26 respectively. this algorithm reduce the delay in each case refer table.2

X SUMMARY AND FUTURE SCOPE

Kogge stone adder Adder is widely used circuit in digital and analog network circuits. adder is base of ALU and microprocessor. kogge stone adder is widely used high performance application[8]. Kogge stone adder can be used in vedic multipliers to calculate the sum of bits An adder is a computerized circuit that does addition of numbers. In numerous PCs and different sorts of processors adders are utilized as a part of the ALUs. They are likewise used in different parts of the processor, where they are utilized to compute addresses, table records, addition and decrement operations, and comparative operations. Tree contain more chains between each stage of propagated and generated carry[5].KGS is parallel form of carry look-a head adder[6].its reduce delay at cost of increase area.[5].KGS has minimum fan-out[9].the maximum fan-out is 2 in all logic level[10].

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