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PHYSICAL LAYER IMPLEMENTATION FOR USB 3.0, WITH LOW POWER 8B/10B ENCODER/DECODER

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ABSTRACT

In this proposed outline it basically incorporates USB 3.0, Physical Layer alongside USB 2.0 usefulness with Super speed usefulness. Physical Layer primarily contains PCI Express and PIPE interface. At present, Universal serial transport (USB) is been gathered as a well known term which is intended to institutionalize the association of PC peripherals to perform correspondence as well as power supply. This project actualizes the DC adjusted 8B/10B coding utilized as a part of Super speed USB. The need of super speed information correspondence prompts to the utilization of USB 3.0. USB 3.0 uses double transport design which gives both Super Speed and non-Super Speed availability. Here, power gets reduced by technique RAM based encoder decoder with modified clock gating.by using this technique power gets reduced by 31.96% at decoder side and 25 % at encoder side. The circuits are designed using verilog HDL . For RTL view and power report of implemented circuit we use Xilinx ISE suite 13.4.

I. INTRODUCTION

Here ,in this project we designed physical layer of USB 3.0 with sufficient power reduction technology which is called **RAM based encoder/decoder with modified clock gating.**

As we know Power consumption plays a major role in present day, 8b/10b encoder and 10b/8b decoder with different low power utilizations philosophies which ensure that adequate moves happen in the bit Stream, so that receiver reliably recover clock and data from bit stream. Here, encoder/decoder is designed by using low power consumption approaches without affecting the purpose of encoding/decoding scheme. In this era of electronics, speed is a crucial factor which has lead to evolution in dual bus architecture technology i.e. USB 2.0 & USB 3.0 can operate simultaneously. 8b/10b encoder and 10b/8b decoder widely used in high speed serial communication standards.

In today's opportunity the VLSI business is developing quickly and it requests for the gadgets which devour less power and there is no effect on their execution. Keeping up the execution with less power utilization is the enormous errand for the specialists. Accordingly, the most extreme time is spent on the power decrease without influencing the execution by the VLSI engineers. There are numerous systems used to diminish the power utilization of the outline.

II UNIVERSAL SERIAL BUS3.0 : REVIEW

It is a determination to set up correspondence between gadgets and a host controller (generally a PC), created and developed by Ajay Bhatt, while working for Intel. USB has viably supplanted an assortment of interfaces for example, serial and parallel ports. USB can associate PC peripherals, for example, mice, consoles, computerized cameras, printers, individual media players, streak drives, Network Connectors, and outer hard drives. For a large portion of those gadgets, USB has turned into the standard association technique.

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2.1 Rendition history

- USB 0.7: Released in November 1994.
- USB 0.8: Released in December 1994.
- USB 0.9: Released in April 1995.
- USB 0.99: Released in August 1995.
- USB 1.0: Released in January 1996
- USB 1.1: Released in September 1998
- USB 2.0: Released in April 2000

In today's opportunity the VLSI business is developing quickly and it requests for the gadgets which devour less power and there is no effect on their execution. Keeping up the execution with less power utilization is the enormous errand for the specialists. Accordingly, the most extreme time is spent on the power decrease without influencing the execution by the VLSI engineers. There are numerous systems used to diminish the power utilization of the outline.

Clock Gating is a procedure utilized for decrease of power in the computerized configuration by clock net. In clock gating method the time is incapacitated at the circumstance where it is most certainly not fundamental, hence this diminishes the power utilization. Clock gating basically turn off the clock where it is pointlessly devours control. By doing this the power utilization is less without influencing the execution of the plan.

The physical layer characterizes the PHY segment of a port and physical association between a downstream confronting port (Host) and upstream confronting port of the gadget . Super speed physical association is the contained two differential information sets transmit and get way. The ostensible information rate is 5GB every second.

In this paper, we have designed physical layer of USB3.0. and reduces the power utilization of the 8b/10b encoder and decoder circuit by using RAM based encoder decoder with modified clock gating. 8B/10B encoder and 10B/8B decoder are broadly utilized due to their low transmission rate and DC remuneration highlight.

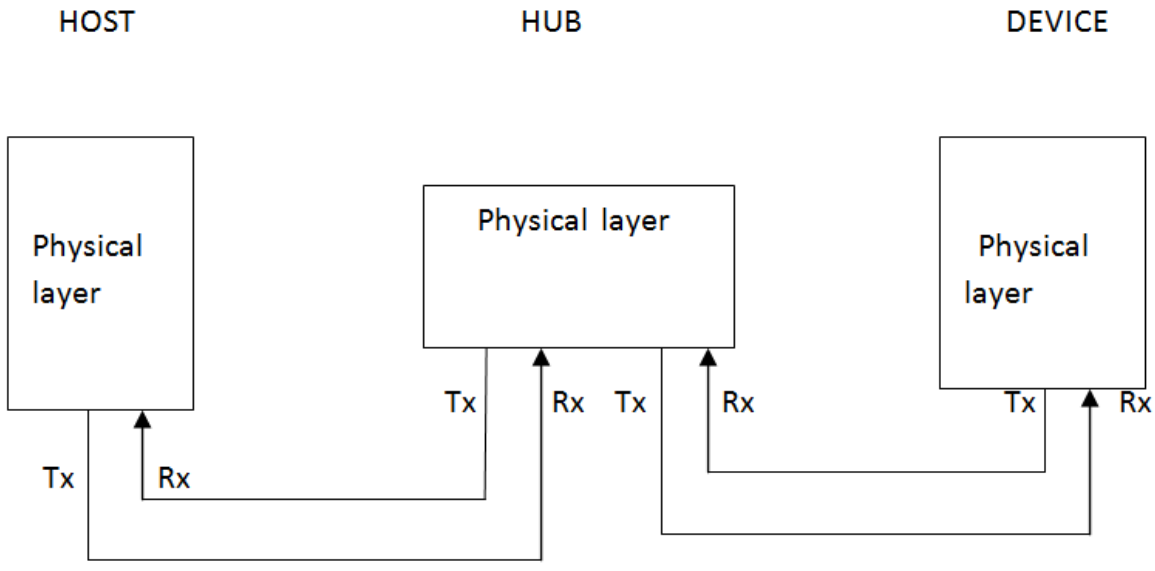

Fig. 1 shows the block diagram of the project work.

International Journal of Electrical and Electronics Engineers
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Transmitter block diagram

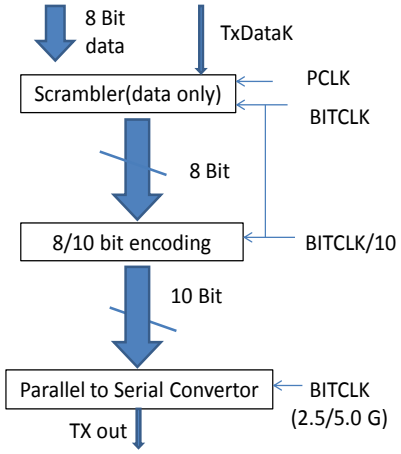

Fig 2 : Transmitter block diagram

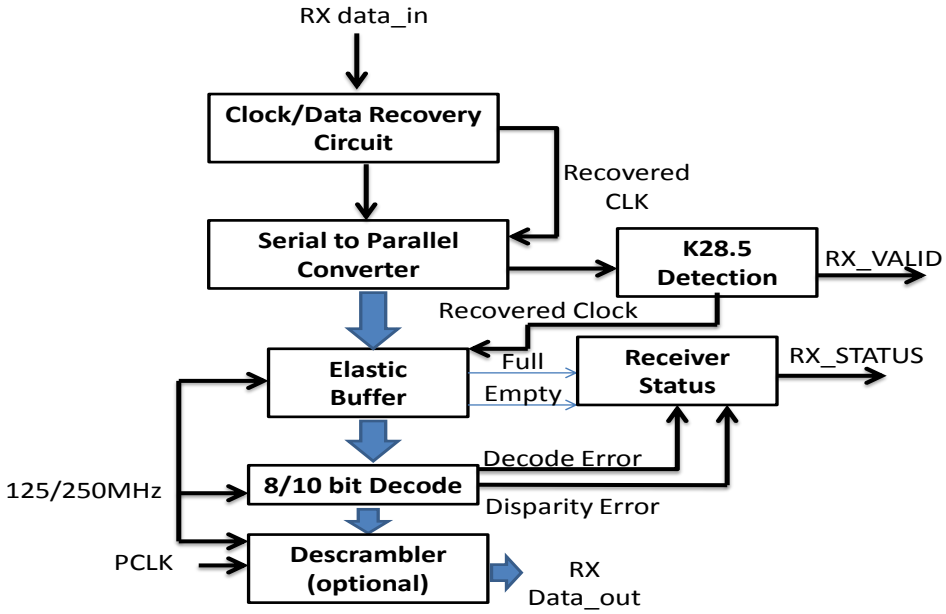

Fig 3 : Receiver block diagram

III. EXISTING WORK

In existing work, 8b/10b encoder and 10b/8b decoder is planned with adequate utilization of innovation called clock gating. Be that as it may, there were some disadavantages. In past framework, an empower stick is given from outside which implies if empower stick is high and information is invalid then it will create a yield then

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this will be checked by beneficiary side and produce a error flag .On account of these two additional pins that is empower stick and error flag stick zone of framework gets expanded and information exchanging likewise gets expanded.

IV. PROPOSED SYSTEM

In modified framework, here Enable pin is produced from inside , so we don't have to take an additional info pin. Presently in light of this pin invalid information is not transmitted from transmitter side, so there is additionally no compelling reason to check the legitimacy of information.

Due to this adjustment number of yield pins gets diminished and territory additionally gets diminished. Furthermore, there is less odds of happening error so mistake flag won't happens. Here, number of ports gets lessened and additional exchanging action gets diminishes and thus dynamic power gets decreased.

Here , we designed RAM based encoder/decoder. There are 256 input conditions, where we have generated a memory in which for all 256 inputs conditions and corresponding 10bit output are stored.

Now whenever 8 bit data is entered at input side rather than calculating the data, it just check the input data in memory and generate an output corresponding to matched value.

4.1 Modified Encoder

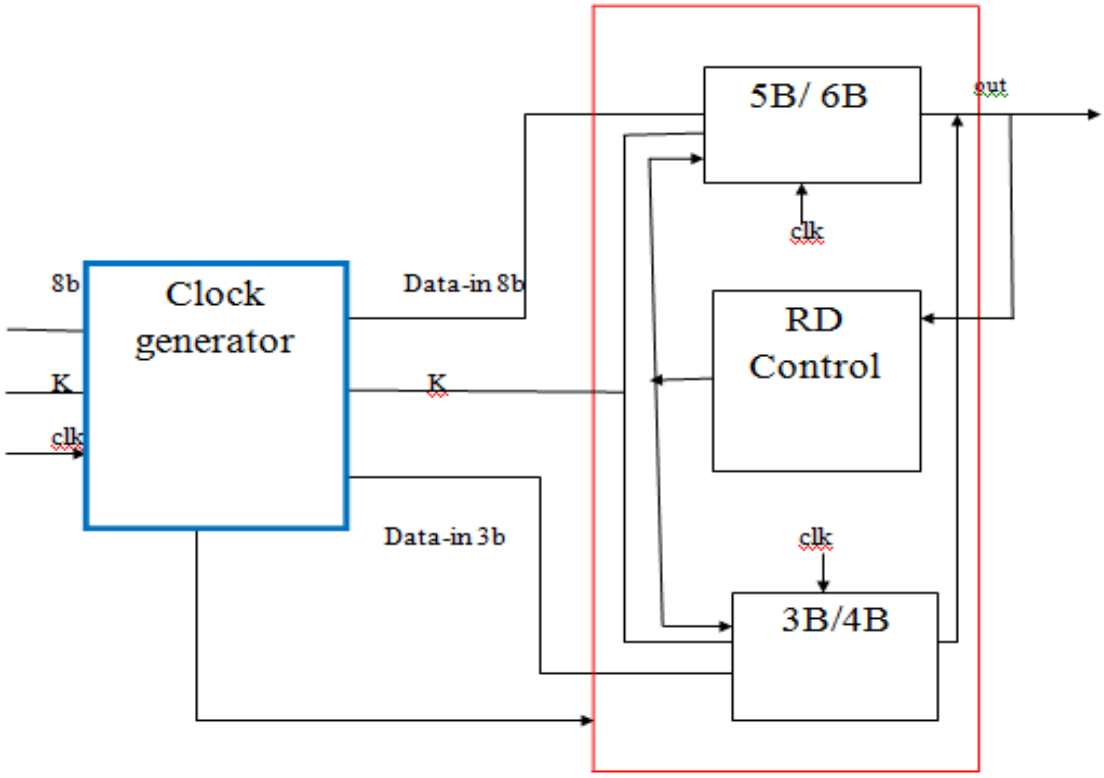

Fig4: Modified architecture of encoder

At first the 8-bit data input goes to clock generator block, this block check, whether the data is valid or not, if input data is valid, it will generate the clock for next module.

At encoder side there are two cases for k=0 and k=1 as demonstrated :

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- If k=0 , then all the 8-bits qualities are valid information.
- If k=1, then 8-bit information entered is taken as summon by the USB and from which just 12 cases are legitimate charge aside from these 12 cases, all information are invalid.

4.2 MODIFIED DECODER

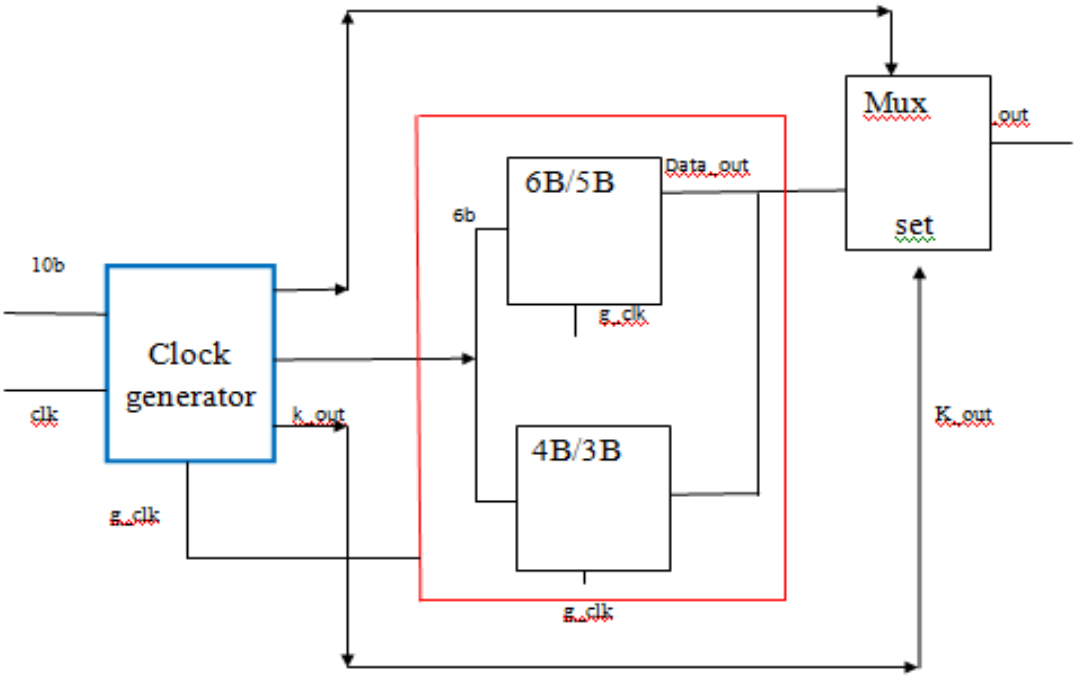

Fig 5 : modified decoder architecture

Here, clock generator checks the validity of data. Then it sends to next module, MUX selects the output between data-out from decoder and code-out from clock generatordepending upon the k-out whether it is 1 or 0 respectively.

At Decoder side , input is of 10 bit that is it can accept 1024 different data but out of 1024 cases only 536 are valid and 488 cases are invalid . these 488 cases will not generate any output and gives the same output as previous output.

V. PERFORMANCE ANALYSIS

In modified waveform at time 2.000ns, k=1, and input data is considered as a command and this input is a valid command, it will generate an output at t=6ns but at time t=6ns , another data is entered, at this time also k=1 but the input data is not valid command therefore it will not generate any output and gives previous data as an output at t=10ns shown in fig.

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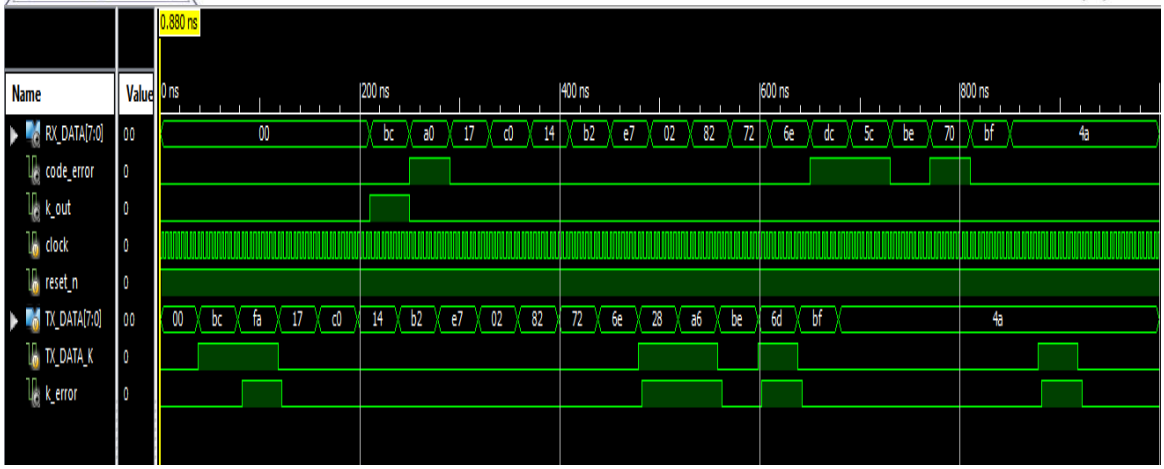

Fig 6: USB3.0 physical layer simulation

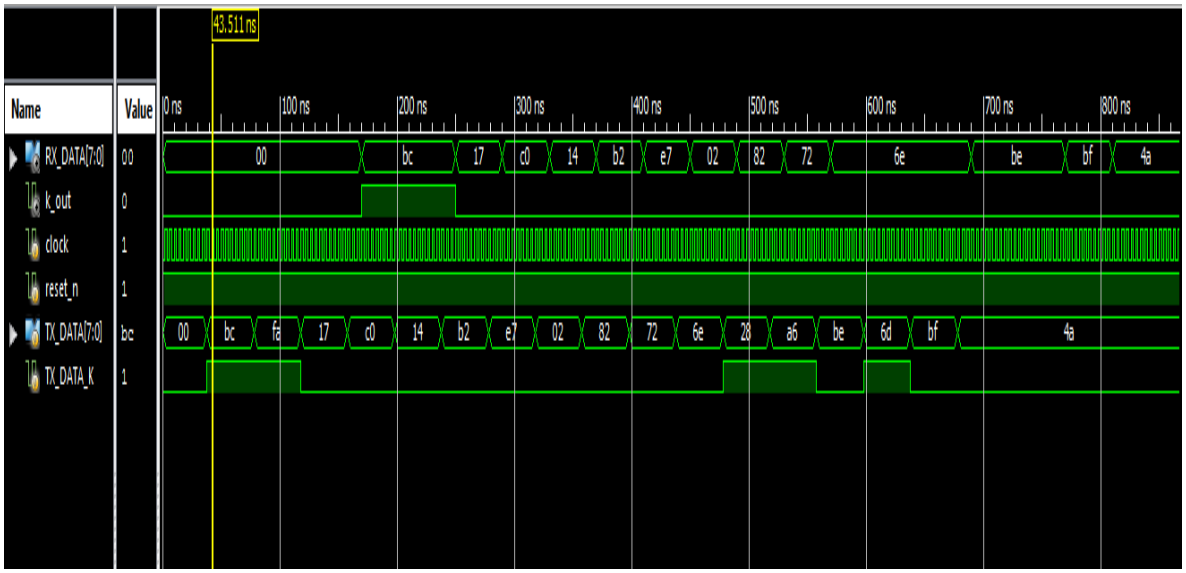

Fig 7: modified USB 3.0 physical layer simulation

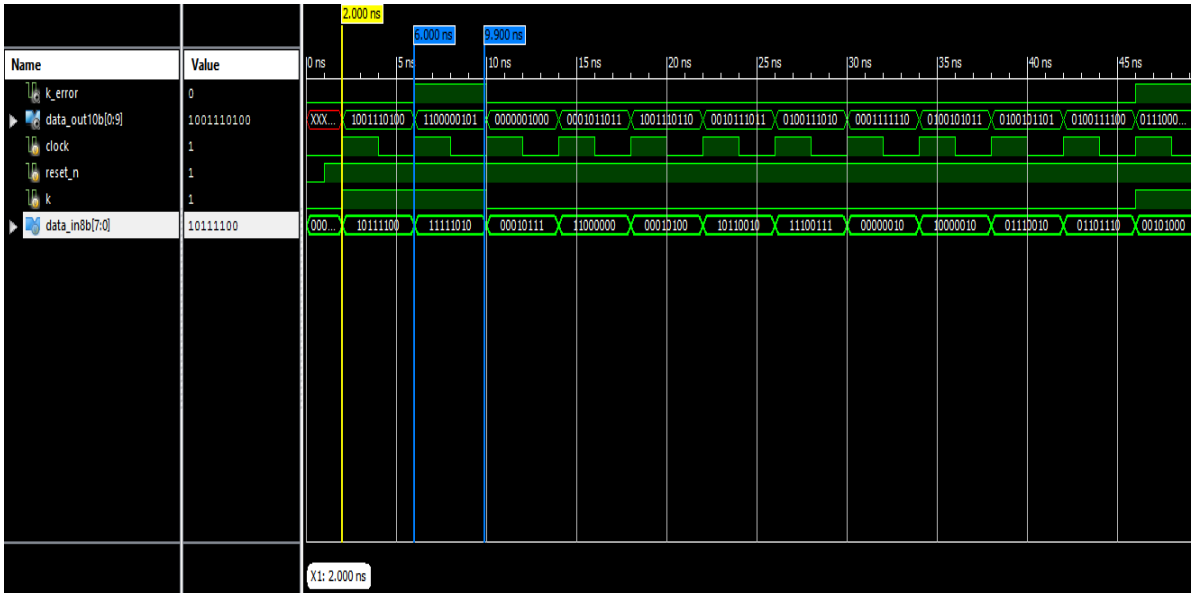

Fig8 : Encoder simulation result

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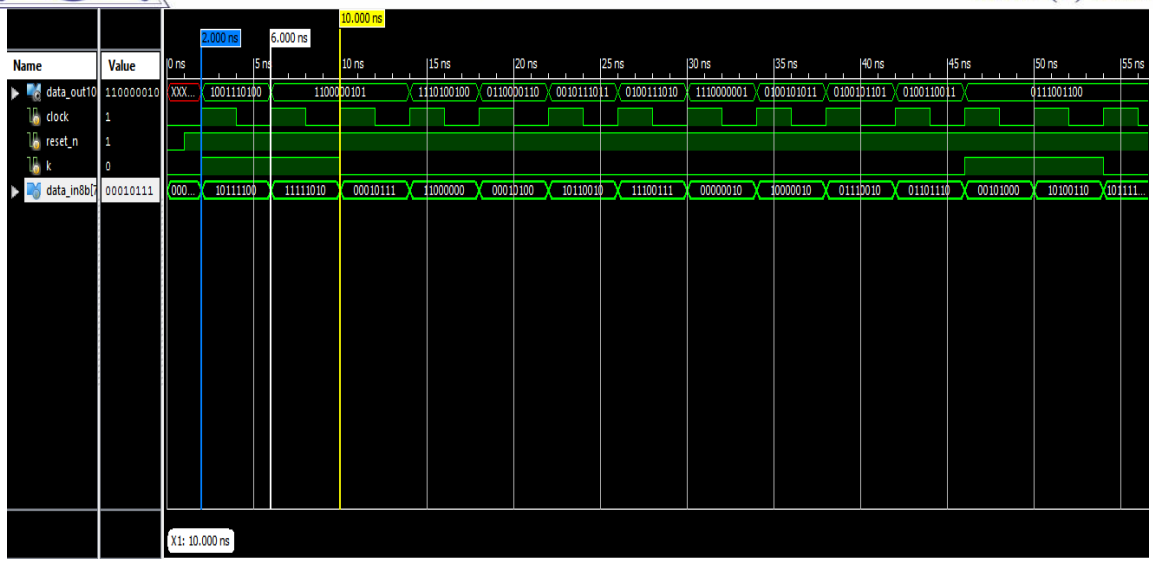

Fig9 : modified Encoder simulation result

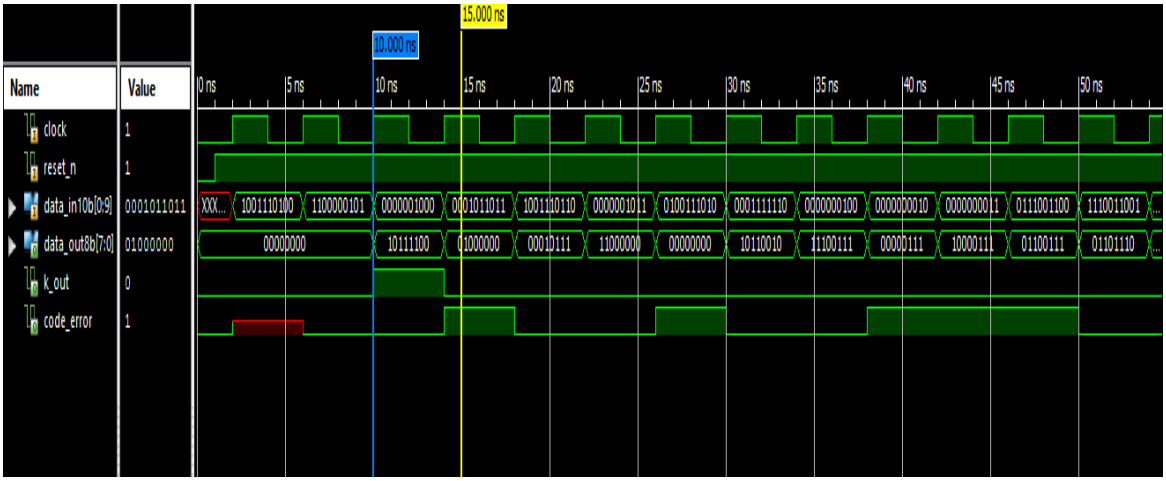

Fig10: decoder simulation result

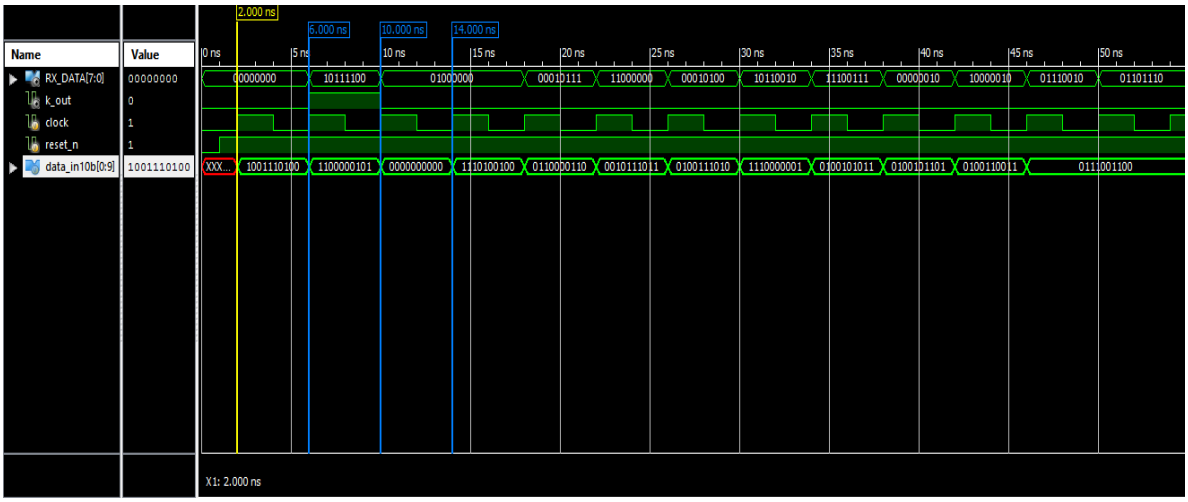

Fig11: Modified decoder result

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VI. EXPERIMENTAL RESULTS

In this paper we have designed a physical layer of USB 3.0 with reduction in power using technology RAM based encoder/decoder with modified clock gating. And power of encoder and decoder is calculated by using this technique and without using this technique. These powers are calculated by using power analyzer of Xilinx ISE suite 13.4.

Powers (mw)		Frequency(Mhz) 250
Encoder	On-chip power	123
	Hierarchy power	510
Encoder using RAM based encoder/decoder with modified clock gating	On chip power	93
	Hierarchy power	283

Table 1: Power COMPARISION of 8B/10B Encoder

Powers(mw)		Frequency(Mhz) 250
Decoder	On-chip power	122
	Hierarchy power	595
Decoder using RAM based encoder/decoder with modified clock gating	On-chip power	83
	Hierarchy power	278

Table.2: Power COMPARISION of 8B/10B Decoder

From our research , we have concluded, the power calculated with RAM based encoder/decoder with modified clock gating is less than without using this technique, we have calculated the power at frequency 250Mhz . for encoder ON CHIP power is reduced by 25%, HIERARCHY power is reduced by 44.5% and for decoder ON CHIP power is reduced by 31.96%, HIERARCHY power is reduced by 53.2%.

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