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# PERFORMANCE EVALUATION OF THE 16X16 BIT MULTIPLIER FOR HIGH SPEED WITH THE USE OF COMPRESSOR ADDER

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**ABSTRACT**

*To perform higher order multiplication large number of adders are required that perform partial product addition and multiplication is one of the most important operation that describes the speed of the processor. In this paper a special kinds of adder has been used that can add up to 19 bits at the same time and the universal method of multiplication i.e. Urdhava-triyakbhyam method derived from ancient Vedas generally known as Vertically and Crosswise technique has been used. For implementation of 16X16 bit Vedic multiplier 32 bit resultant equations have been calculated using vertically and crosswise technique and compressor adder used to implement these equations. The designs are coded in VHDL and synthesized using Xilinx ISE 14.6 using Spartan 3e series of FPGA. The combinational delay calculated for 16X16 Vedic multiplier is 29.506ns that clearly indicate better performance of Vedic multiplier.*

***Keywords: Compressor adder, Vedic Mathematics, Urdhava-triyakbhyam sutra.***

## I. INTRODUCTION

We all use smart phones that are inbuilt with latest features but sometimes we face situation where our phone gets hang or display message like system not responding the reasons behind it is the speed of the processor and the speed of the processor merely depends on how fast it is performing the multiplications as all data processing multiplication involve multiplication so multiplication is the building block operation that describes the speed. In recent years speed, power and area is the main concern in VLSI domain. The Urdhava-triyakbhyam sutra used in this paper is derived from ancient Vedas this sutra is universal method of multiplication it is chosen as the delay with the increase in number of input is less as compared to other sutras it adds binary numbers and digits vertically and crosswise and adds them with the help of adder. The method has been explained below:

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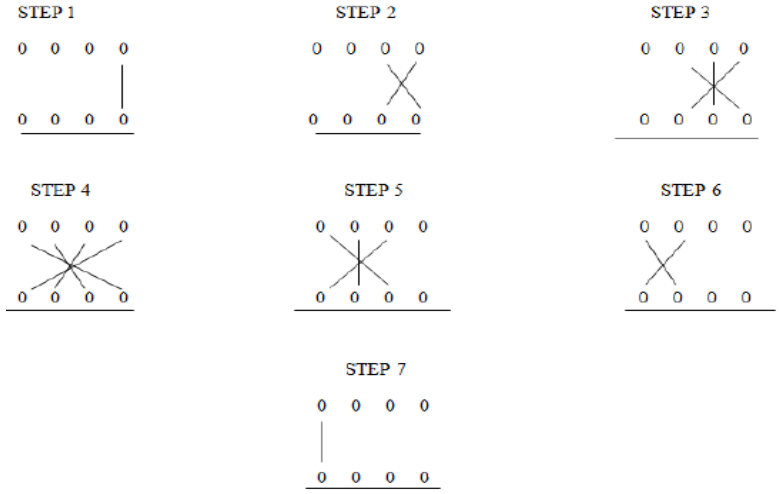


**Fig.1. 4X4 Bit multiplication with vertically and Crosswise technique [1]**

This paper compromises of four sections. Section I describes introduction. Section II compressor adders. Section III is implementation and equations. Section IV Tables and simulation results.

## II. COMPRESSOR ADDER

In this paper five compressor adder has been used they are 5X3, 7X4, 10X4, 15X4, 20X5 compressor adder for the addition of partial product that are produced during multiplication of 16x16 Vedic multiplier. Each of their architecture has been discussed below:

### 2.1. 5-3 compressor adder

As the name indicates it takes five bit input at the same time and gives three bit resultant. If we are considering all the inputs to be 1 then the maximum output can be 101. We have basically two architecture of 5-3 compressor adder one is traditional that make use of only half adders and full adders and other is conventional or modified that make use MUX.

Its structure consist of two full adders and two half adders in traditional one and in modified three 4:1 MUX is used which allow the use of lesser XOR gates and high speed.

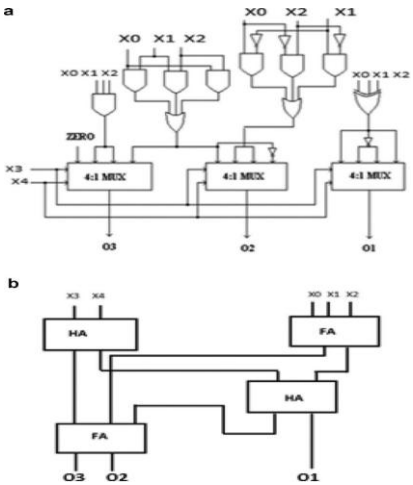


**Fig.2 (a) Modified design for 5-3 compressor (b) 5-3 compressors with full adders and half-adders [2]**

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### 2.2 7-4 Compressor adder

It takes seven input at a same time and gives four bit resultant. If all the input are 1 then maximum output can be obtained is 0110. Its structure compromises of one 5-3 compressor adder , two half adders, one full adder and a combinational circuit of AND and XOR gate having same input i.e. $X_5$,$X_6$. Its architecture has been given below:

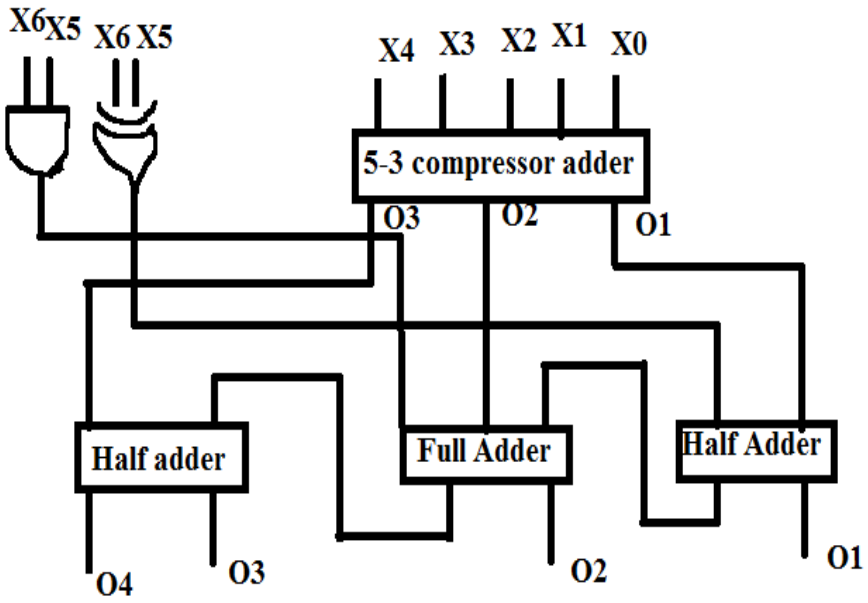


**Fig.3. 7-4 compressor adder with use of 5-3 compressor adder and full adder.**

### 2.3 10-4 compressor adder

It takes ten input at a time and four bit resultant can be obtained and maximum of 1010 resultant can be obtained. Its circuitry consists of two 5-3 compressor adder, two full adders and a half adder.

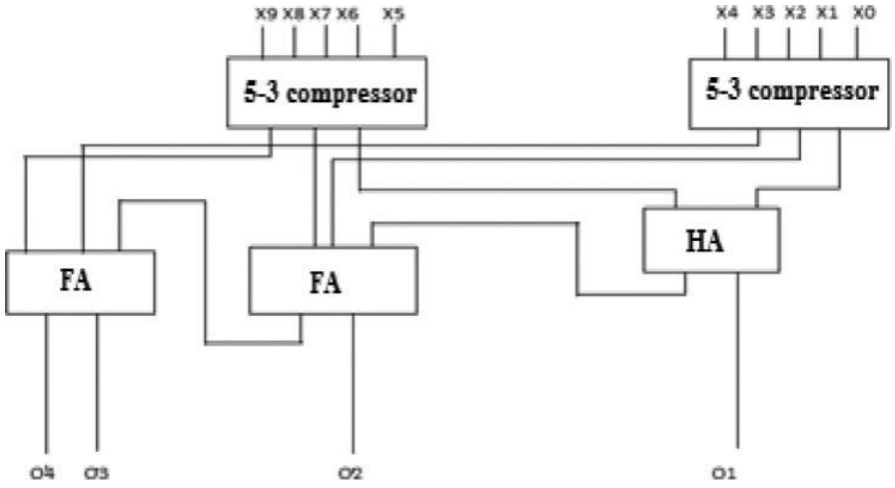


**Fig.4. 10-4 compressor adder with use of 5-3 compressor adder and full adder, half adder[2]**

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### 2.4 . 15-4 compressor adder

In this fifteen input can be taken at one time and four bit resultant can be obtained and maximum resultant can be of 1111. Its circuitry consists of two 5-3 compressor adders, five full adders and one 4 bit parallel adder. As it is using modified design of 5-3 compressor adder so delay is less.

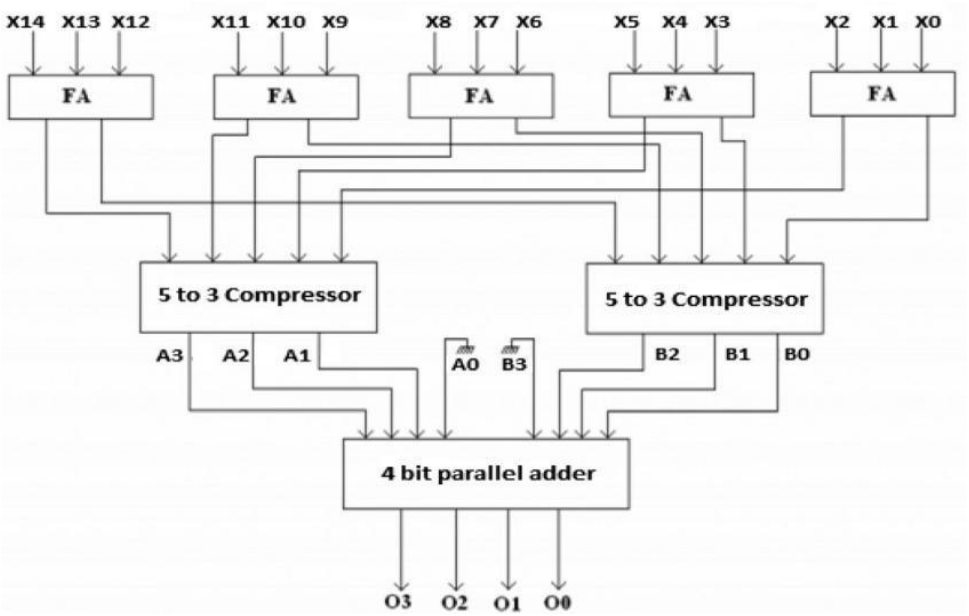


**Fig.5. 15-4 compressor adder with use of 5-3 compressor adder and full adder[2]**

### 2.5 . 20-5 compressor adder

In this twenty inputs can be taken at one time and 5 bit resultant can be obtained and maximum resultant can be obtained be of 10010. Its circuitry consists of one 15-4 compressor adder, one 5-3 compressor adder, two full adders and two half adders.

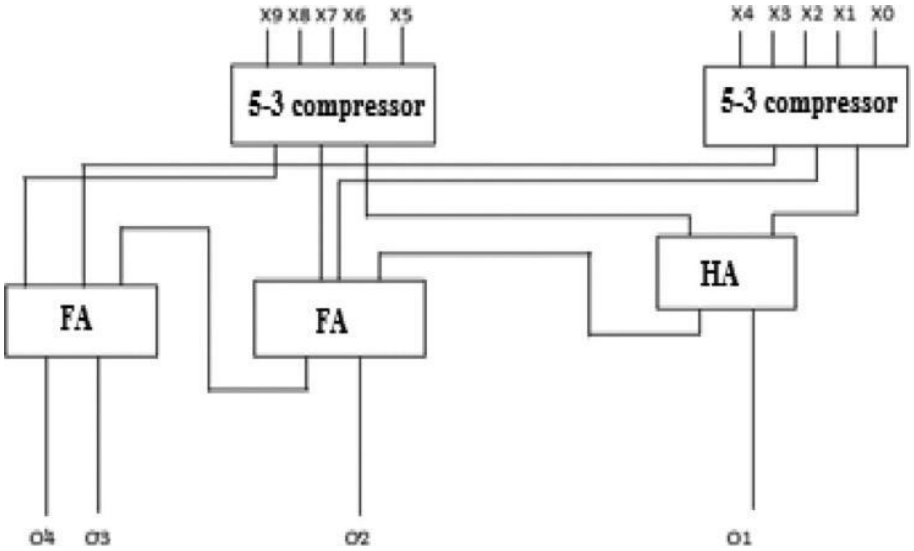


**Fig.6. 20-5 compressor adder with use of 15-4 compressor adder and full adder[2]**

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## III. EQUATIONS TO BE IMPLEMENTED

Let both the numbers be 16 bit long i.e. a= $a16a14a13a12a11a10a9a8a7a6a5a4a3a2a1a0$ and second is

b= $b16b14b13b12b11b10b9b8b7b6b5b4b3b2b1b0$ and their product 'r' is 32 bit i.e. ($r31-0$) and carry signal will be $c1 - c89$.

Equations that are going to be implemented are as follow:

$s_0 = a_0b_0$

$c_1s_1 = a_0b_1 + a_1b_0$

$c_3c_2s_2 = c_1 + a_0b_2 + a_1b_1 + a_2b_0$

$c_5c_4s_3 = c_2 + a_0b_3 + a_1b_2 + a_2b_1 + a_3b_0$

$c_7c_6s_4 = c_4 + c_3 + a_0b_4 + a_1b_3 + a_2b_2 + a_3b_1 + a_4b_0$

$c_{10}c_9c_8s_5 = c_6 + c_5 + a_0b_5 + a_1b_4 + a_2b_3 + a_3b_2 + a_4b_1 + a_5b_0$

$c_{13}c_{12}c_{11}s_6 = c_8 + c_7 + a_0b_6 + a_1b_5 + a_2b_4 + a_3b_3 + a_4b_2 + a_5b_1 + a_6b_0$

$c_{16}c_{15}c_{14}s_7 = c_{11} + c_9 + a_0b_7 + a_1b_6 + a_2b_5 + a_3b_4 + a_4b_3 + a_5b_2 + a_6b_1 + a_7b_0$

$c_{19}c_{18}c_{17}s_8 = c_{10} + c_{12} + c_{14} + a_0b_8 + a_1b_7 + a_2b_6 + a_3b_5 + a_4b_4 + a_5b_3 + a_6b_2 + a_7b_1 + a_8b_0$

$c_{22}c_{21}c_{20}s_9 = c_{17} + c_{15} + c_{13} + a_0b_9 + a_1b_8 + a_2b_7 + a_3b_6 + a_4b_5 + a_5b_4 + a_6b_3 + a_7b_2 + a_8b_1 + a_9b_0$

$c_{25}c_{24}c_{23}s_{10} = c_{20} + c_{18} + c_{16} + a_0b_{10} + a_1b_9 + a_2b_8 + a_3b_7 + a_4b_6 + a_5b_5 + a_6b_4 + a_7b_3 + a_8b_2 + a_9b_1 + a_{10}b_0$

$c_{28}c_{27}c_{26}s_{11} = c_{23} + c_{21} + c_{19} + a_0b_{11} + a_1b_{10} + a_2b_9 + a_3b_8 + a_4b_7 + a_5b_6 + a_6b_5 + a_7b_4 + a_8b_3 + a_9b_2 + a_{10}b_1 + a_{11}b_0$

$c_{32}c_{31}c_{30}c_{29}s_{12} = c_{26} + c_{24} + c_{22} + a_0b_{12} + a_1b_{11} + a_2b_{10} + a_3b_9 + a_4b_8 + a_5b_7 + a_6b_6 + a_7b_5 + a_8b_4 + a_9b_3 + a_{10}b_2 + a_{11}b_1 + a_{12}b_0$

*C36C35C34C33S13 =C29 + C27 + C25 + a0b13 + a1b12 + a2b11 + a3b10 + a4b9 + a5b8 + a6b7 + a7b6 + a8b5 + a9b4 + a10b3 + a11b2 + a12b1 + a13b0*

*C40C39C38C37S14 = C33 + C30 + C28 + a0b14 + a1b13 + a2b12 + a3b11 + a4b10 + a5b9 + a6b8 + a7b7 + a8b6 + a9b5 + a10b4 + a11b3 + a12b2 + a13b1 + a11b0*

*C44C43C42C41S15 = C37 + C34 + C31 + a0b15 + a1b14 + a2b13+ a3b12+ a4b11+ a5b10+ a6b9+ a7b8+ a8b7 + a9b6 + a10b5 + a11b4 + a12b3 + a13b2 + a14b1+ a15b0*

C48C47C46C45S16 = C32 + C35 + C33+ a0b15 + a1b14 + a2b13 + a3b12 + a4b11 + a5b10 + a6b9 + a7b8 +a8b7 +a9b6 + a10b5 + a11b4 + a12b3 + a13b2 + a14b1 + a15b0

C52C51C50C49S17 = C45 + C42 + C39+ C36+ a2b15+ a3b14+ a4b13+ a5b12+ a6b11+ a7b10+ a8b9+ a9b8 +a10b7+a11b6 + a12b5 + a13b4 + a14b3 + a15b2

C56C55C54C53S18 = C49 + C43 +C46+ C40+ a3b15+ a4b14+ a5b13+ a6b12+ a7b11+ a8b10+ a9b9+ a10b8 +a11b7+a12b6 + a13b5 + a14b4 + a15b3

C60C59C58C57S19= C53 + C50 +C47+ C44+ a4b15+ a5b14+ a6b13+ a7b12+ a8b11+ a9b10+ a10b9 +a11b8 +a12b7+a13b6 + a14b5 + a15b4

*C*63*C*62*C*61*S*20= C57 + C54 +C51+ C4 8+ a5b1 5+ a6b14 + a7b13+ a8b12+ a9b11+ a10b10 + a11b9 + a12b8 + a13b7+a14b6 + a15b5

*C*66*C*65*C*64*S*21= C61 + C58 + C55+ C45 + a6b1 5+ a7b14 + a8b13+ a9b12+ a10b11+ a11b10 + a12b9 + a13b8 + a14b7+a15b6

*C*69*C*68*C*67*S*22= C56 + C59 + C62+ C64 + a6b1 5+ a7b14 + a8b13+ a9b12+ a10b11+ a11b10 + a12b9 + a13b8 + a14b7+a15b6

*C*72*C*71*C*70*S*23= C67+ C65 + C63+ C60+ a8b1 5+ a9b14 + a10b13+ a11b12+ a12b11+ a13b10 + a14b9+a15b8

*C*75*C*74*C*73*S*24= C70+ C68 + C66+ a9b1 5+ a10b14 + a11b13+ a12b12+ a13b11+ a14b10 + a15b9

*C*78*C*77*C*76*S*25= C70+ C68 + C66+ a10b1 5+ a11b14 + a12b13+ a13b12+ a14b11+ a15b10

*C81C80C79S26= C76+ C76 + C72+ a11b1 5+ a12b14 + a13b13+ a14b12+ a15b11*

*C32C33S27= C79+ C77 + C75+ a12b1 5+ a13b14 + a14b13+ a15b12*

*C85C84S28= C82+ C80 + C78+ a13b1 5+ a14b14 + a15b13*

*C87C86S29= C84+ C83 + C81+ a14b1 5+ a15b14*

*C88S30= C85+ C86 + a15b15*

As for these equations we require adders which can add 2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19 bits at same time so the compressor adders come into play. The structure of compressor adders has been given below we have used 5-3, 10-4, 15-4 and 20-5 compressor adder.

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## IV. RESULTS

The designs are coded in VHDL and synthesized using Xilinx ISE 14.6 simulator and family used is XILINX: SPARTAN 3E:XC3S500E FG3200, speed grade -4. Results are clearly indicating better speed performance. Table 1 is tabulated with the comparison results of combinational delay of modified compressor adder with traditional ones. Table 2 is tabulated with the comparison results of combinational delay of array, Wallace and booth tree multiplier [2] with our purposed multiplier.

| Input bits | Traditional adder delay | Modified adder delay |
|---|---|---|
| 5 | 5.57 | 5.570 |
| 7 | 6.768 | |
| 10 | 6.875 | 6.787 |
| 15 | 7.953 | 7.953 |
| 20 | 8.325 | 8.235 |

TABLE 1. Comparison table of combinational delay of traditional and modified compressor adder

| 16 bit multiplier | Combinational delay | % improvement |
|---|---|---|
| Array multiplier | 43.946 | |
| Wallace tree multiplier | 46.046 | |
| Booth multiplier | 37.041 | |
| multiplier in base paper | 32 | |
| Purposed multiplier | 29.506 | 10 |

TABLE 2. Comparison table of combinational delay of 16 bit Vedic multipliers

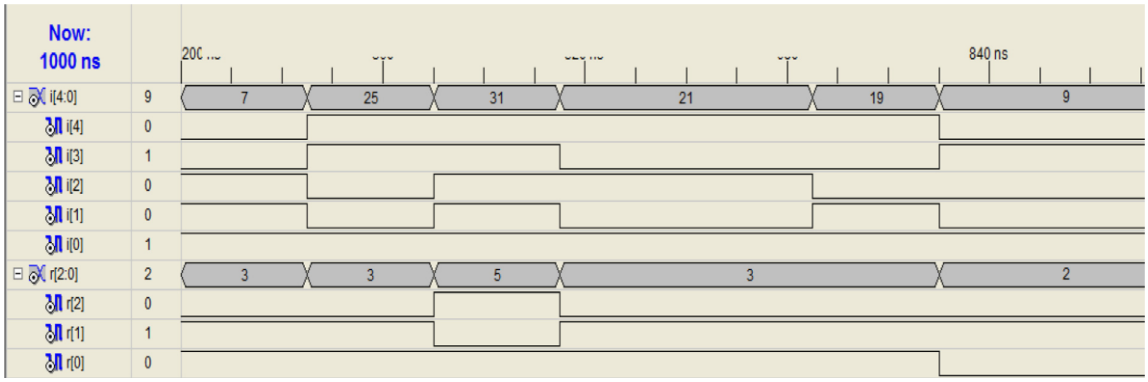


**Fig.7. simulation results of 5-3 compressor adder**

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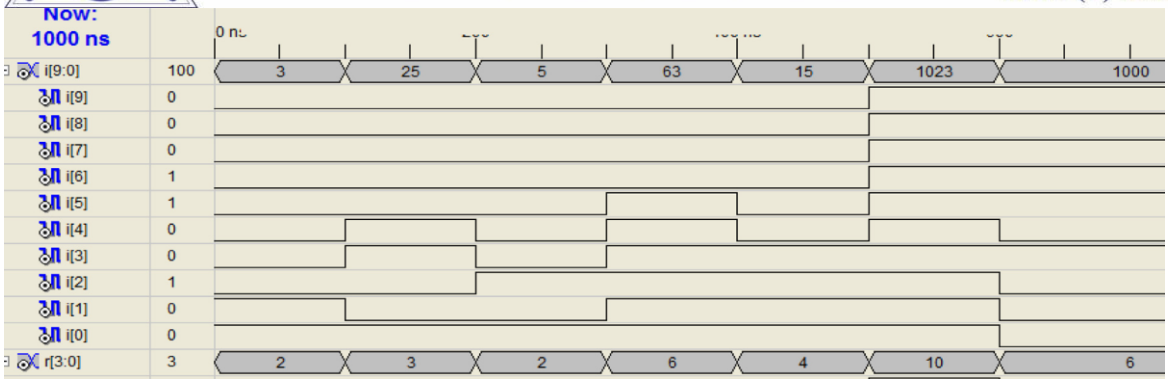


**Fig.8. simulation results of 10-4 compressor adder**

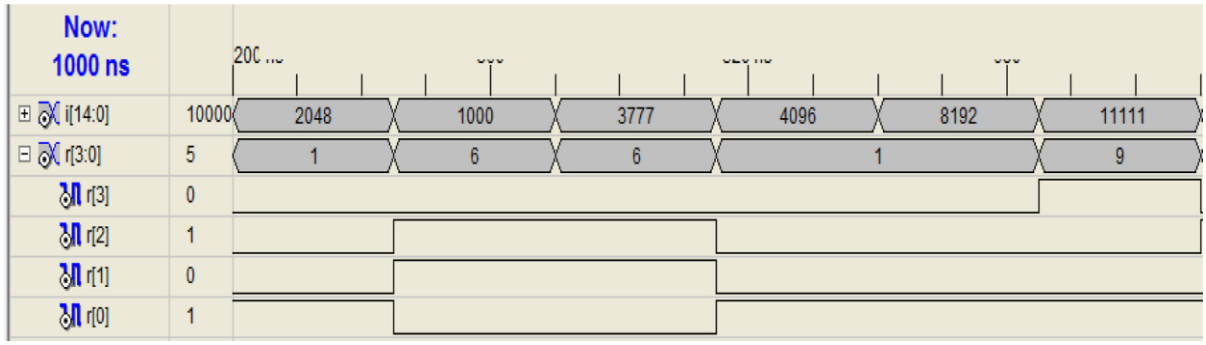


**Fig.9. simulation results of 15-4 compressor adder**

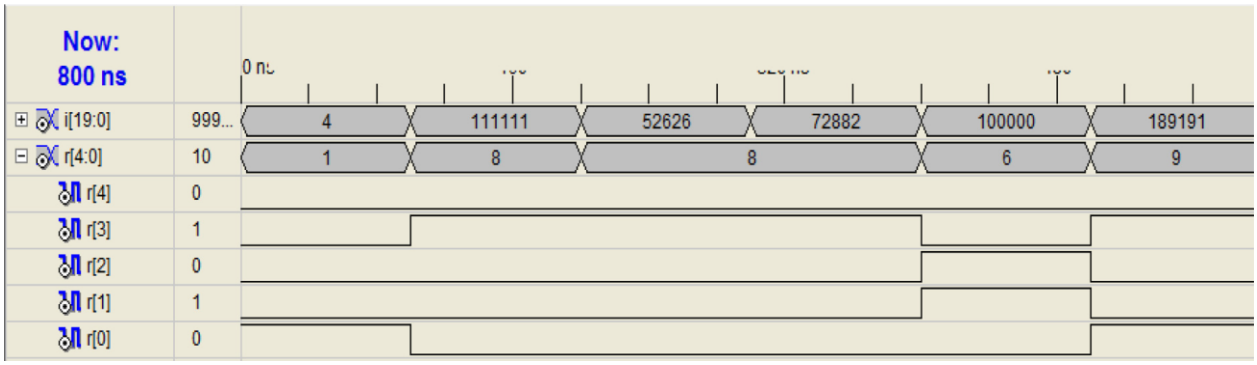


**Fig.10. simulation results of 20-5 compressor adder**

## V. CONCLUSION AND FUTURE SCOPE

Using compressor not only decreases the critical delay but also reduces the stage operation simultaneously. It can be used where stringent demands of speed are required. It can be a great use in digital signal processing applications. As the parallel generation of partial products are generated and unwanted multiplication steps has been removed so speed increases which was the main concern. 16 bit multiplier uses the entire compressors adder effectively for partial product reduction.

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