International Journal of Electrical and Electronics Engineers
Vol. No. 9, Issue No. 01, January-June 2017
ISSN (O) 2321-2055
ISSN (P) 2321-2045

DENOISING OF EOG SIGNAL USING DISCRETE WAVELET TRANSFORM BASED ON THE DAUBECHIES ARCHITECTURE

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ABSTRACT

The Denoising of Electrooculogram (EOG) signals is of practical importance in medical diagnosis. In this paper an effort is made for denoising of the EOG signal by using Discrete Wavelet Transform (DWT). The DWT is implemented using an Modified daubechies architecture. Also the performance comparison of this architecture with other existing architecture is evaluated. The implementation resulted in a better denoised EOG signal with signal to noise ratio of 31.1630 dB and minimum mean square error of 0.0456.

Keywords: EOG signal; Denoising; thresholding; modified daubechies architecture.

I. INTRODUCTION

Electrooculography is a technique for measuring the resting potential of an eye and the resulting signal called Electrooculogram (EOG) signal. The signal gives different patterns for different eye movements. The eye movement is measured by skin electrodes which are placed above, below, left and right with an additional reference electrode is placed on the forehead[1]. This paper is described of four sections. First section gives introduction, base line drift removal of EOG signal is explained in second section, DWT Denoising method explained in third section and fourth section discusses about modified daubechies architecture architecture.

II. BASE LINE DRIFT REMOVAL

Small changes in EOG signal is called baseline drift that are not related to the movements of eye. Electrode polarization, interfering background signals etc., are sources of this baseline drift [2]. Here modified daubechies architecture is applied for removing this drift.

III. DWT DENOISING METHOD

The EOG signal is generally corrupted by base line drift noise. The wavelet denoising technique will reduce the noise and preserve the signal. The small wavelet coefficients are adjusted by using thresholding technique. In the thresholding technique the detail output greater than the threshold value are stored and the remaining are made zero[3]. The flowchart for the DWT based denoising is shown in Fig. 1

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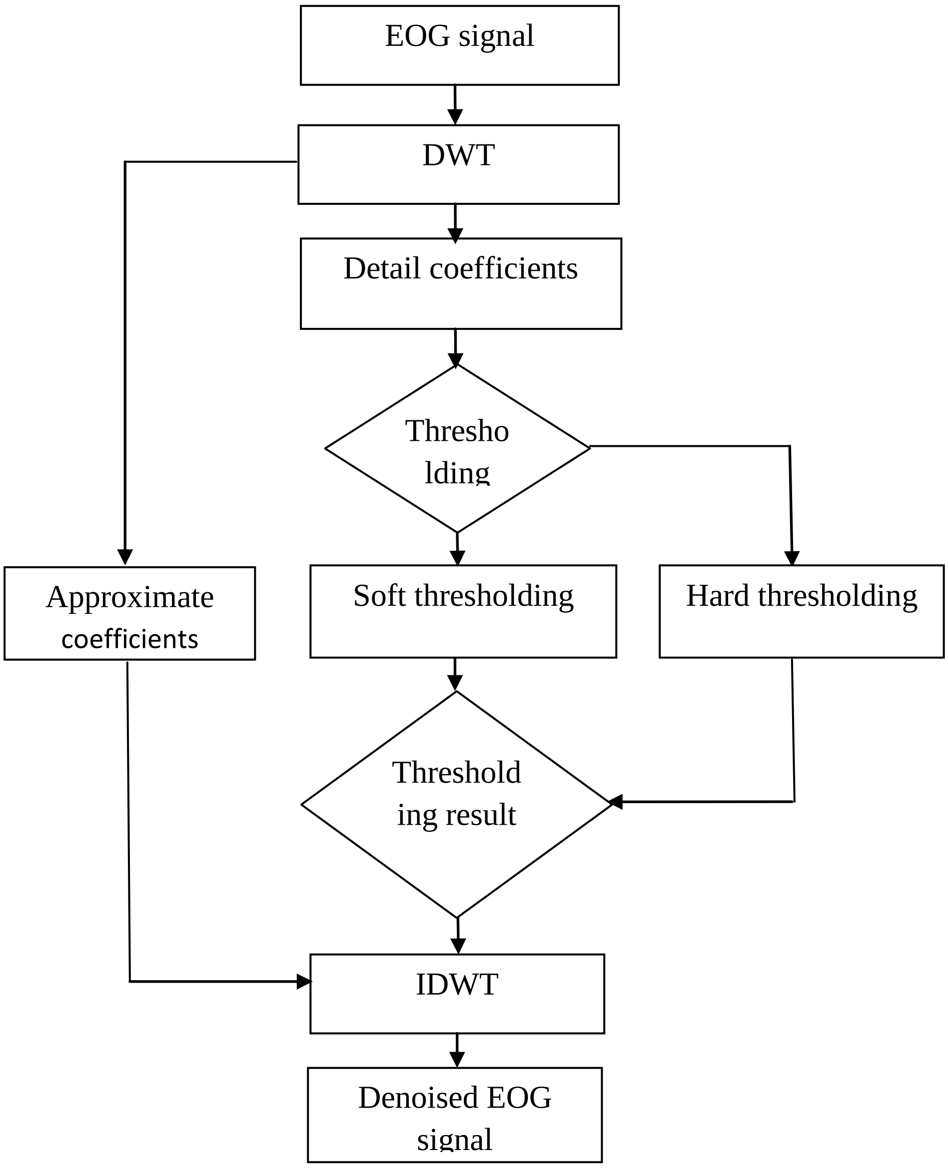

Fig1:noise removal method using DWT

And the threshold value is computed using the equation (1)

$$\theta = \sigma\sqrt{2\log(s)} \qquad \textbf{(1)}$$

where θ is the threshold, σ is the standard deviation; S is the number of samples. The inverse DWT processes the threshold coefficients to reconstruct the original EOG signal.

IV.MODIFIED DAUBECHIES 1-D ARCHITECTURE FOR HIGH/LOW PASS FILTER:

The proposed design, named ZXY, has two stages as simple as Daubechies architecture as shown in fig2. The operations are scheduled and assigned into two pipeline stages: a multiplier block and an adder block. In the first stage, the two input data are simultaneously multiplied by all coefficients. The second stage is the adder block which executes in order of formula on the right clock. Here, the multipliers and the adders, used in the high-pass filter and the low-pass filter. As an example, the 7-tap high-pass filter of the proposed 1-D 9/7-tap DWT is shown in fig2 . In the first stage, the multipliers use the coefficients from 9/7 Daubechies filter. Because of the repeated coefficients (g1, g2, and g3), the proposed 7-tap highpass filter uses less three multipliers than the original Daubechies architecture of fig2. Similarly, the 9-tap low-pass filter uses less four multipliers than the original Daubechies architecture. The second stage uses 6 adders which parallelly execute the data from the first- and second- pipeline stages. The latency of the first stage is one multiplier delay, and the latency of the second stage is two adder delays. Therefore, the pipeline clock is determined from the maximum delay of either one multiplier or two adders.

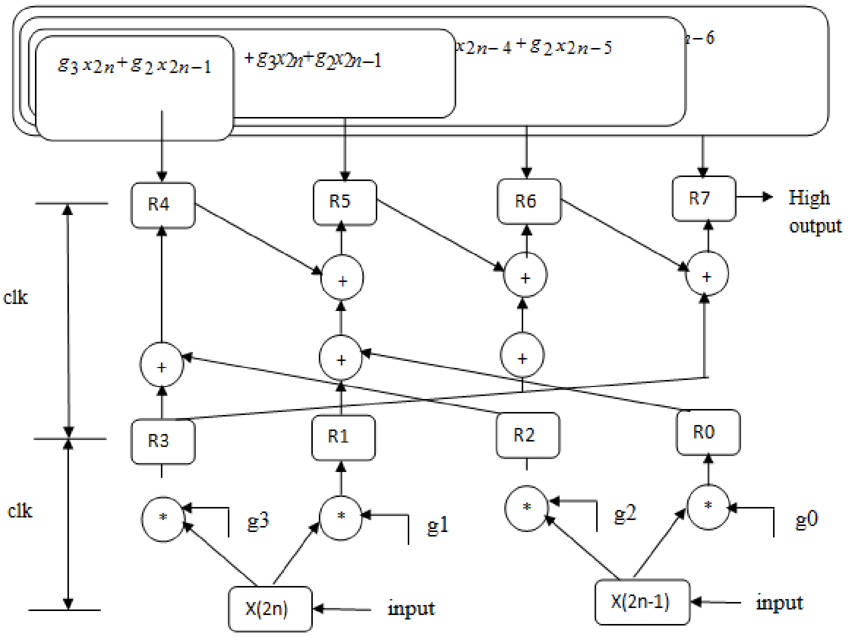

Fig2: The proposed DWT architecture for 7-tap high-pass filter

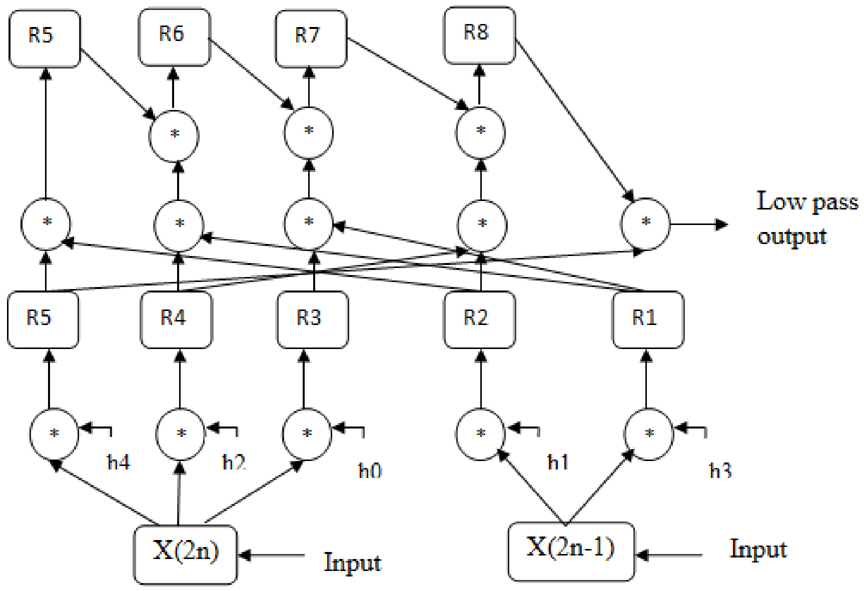

Fig3: The proposed DWT architecture for 9-tap low-pass filter

The proposed architecture has the similar structure as the general transposed FIR filter. However, the clock cycle of the pipeline version of the transposed FIR filter is constrained by one multiplier delay plus one adder delay as Figure3

clk	R3	R2	R1	R0	(next clk) R4=R3+R2	(next clk) R5=R4+R1+R0
1	g_3x_1	g_2x_2	g_1x_1	g_0x_2	0	0
2	g_3x_3	g_2x_4	g_1x_3	g_0x_4	$g_3x_1+ g_2x_2$	$g_1x_1+ g_0x_2$
3	g_3x_5	g_2x_6	g_1x_5	g_0x_6	$g_3x_3+ g_2x_4$	$g_3x_1+g_2x_2+g_1x_3+g_0x_4$
4	g_3x_7	g_2x_8	g_1x_7	g_0x_8	$g_3x_5+ g_2x_6$	$g_3x_3+g_2x_4+g_1x_5+g_0x_6$
5	g_3x_9	g_2x_{10}	g_1x_9	g_0x_{10}	$g_3x_7+ g_2x_8$	$g_3x_5+g_2x_6+g_1x_7+g_0x_8$
6	g_3x_{11}	g_2x_{12}	g_1x_{11}	g_0x_{12}	$g_3x_9+ g_2x_{10}$	$g_3x_7+g_2x_8+g_1x_9+g_0x_{10}$
7	g_3x_{13}	g_2x_{14}	g_1x_{13}	g_0x_{14}	$g_3x_{11}+g_2x_{12}$	$g_3x_9+g_2x_{10}+g_1x_{11}+g_0x_{12}$

Table 1: The dataflow for the ZXY 7-tap high-pass filter for registersR0-R5

Clk	(Next clk) R6=R5+R1+R2	(Next clk) R7=R6+R3
1	0	0
2	$g_1x_1+g_2x_2$	g_3x_1
3	$g_1x_1+g_0x_2+g_1x_3+g_2x_4$	$g_1x_1+g_2x_2+g_3x_3$
4	$g_3x_1+g_2x_2+g_1x_3+g_0x_4+g_1x_5+g_2x_6$	$g_1x_1+g_0x_2+g_1x_3+g_2x_4+g_3x_5$
5	$g_3x_3+g_2x_4+g_1x_5+g_0x_6+g_1x_7+g_2x_8$	$g_3x_1+g_2x_2+g_1x_3+g_0x_4+g_1x_5+g_2x_6+g_3x_7$
6	$g_3x_5+g_2x_6+g_1x_7+g_0x_8+g_1x_9+g_2x_{10}$	$g_3x_3+g_2x_4+g_1x_5+g_0x_6+g_1x_7+g_2x_8+g_3x_9$
7	$g_3x_7+g_2x_8+g_1x_9+g_0x_{10}+g_1x_{11}+g_2x_{12}$	$g_3x_5+g_2x_6+g_1x_7+g_0x_8+g_1x_9+g_2x_{10}+g_3x_{11}$
8	$g_3x_9+g_2x_{10}+g_1x_{11}+g_0x_{12}+g_1x_{13}$ $+g_2x_{14}$	$g_3x_7+g_2x_8+g_1x_9+g_0x_{10}+g_1x_{11}+g_2x_{12}+g_3x_{13}$

Table 2: the dataflow for the ZXY 7-tap high-pass filter for registers R6-R7

The proposed architecture uses different resources for even and odd number of filter taps. The odd-number-tap filter can reduce some multipliers of coefficients, whereas the even number- tap filter can reduce some adders. The detailed comparison results in general taps are listed in Table.2. The even-number-tap filter is designed as the same way as 4-tap DWT.

In Fig2, the proposed structure shows a two-stage pipeline with the pipeline stage delay (the inverse of throughput) constraint of two adders at every clock. In Figure3, the lifting structure shows one stage pipeline with the pipe stage delay constraint of one multiplier plus two adders at every clock.

V. ESTIMATION OF MEAN SQUARE ERROR (MSE) AND SIGNAL TO NOISE RATIO (SNR)

The Mean Square Error (MSE) is the one of the best parameter to measure the reconstructed signal. It represents the mean squared error between the de noised signal and the reference signal and is given by

- Mean square error (MSE) : is represents the error between denoised signal and reference signal.

$$MSE = \frac{1}{n}\sum_{i=1}^{n}\left[X(i) - X_d(i)\right]^2 \qquad (2)$$

n = length of the signal

X = the reference signal

X_d =the denoised signal

- Root mean square error (RMS):

$$RMSE = \sqrt{MSE} \qquad (3)$$

- Signal to noise ratio (SNR):

$$SNR = 10\log\frac{\sum_{i=1}^{N} x(i)^2}{\sum_{i=1}^{N}\left(x(i) - \bar{x}(i)\right)^2} \qquad (4)$$

MSE, RMSE and SNR of Modified Daubechies wavelet transform:

A comparison of design implementation summary is presented for modified Daubechies and existing Daubechies architecture is presented in the Table

VII. RESULTS AND DISCUSSION

The mean square error (MSE), root mean square error (RMSE) and signal to noise ratio (SNR) valuesare computed and are shown in Table 3. The reference and denoised EOG signals in MATLAB simulation is shown in Fig.4 and Fig.5 respectively.

Name of the architecture	Mean square error (MSE)	Root mean square error (RMS)	Signal to noise ratio (SNR) in db
Modified daubechies architecture	0.0456	0.2135	31.1630
Sym8	0.0552	0.2350	29.2440
Coeff3	0.0461	0.2147	31.0523

Table 3: MSE,RMSE and SNR of Modified Daubechies wavelet transform

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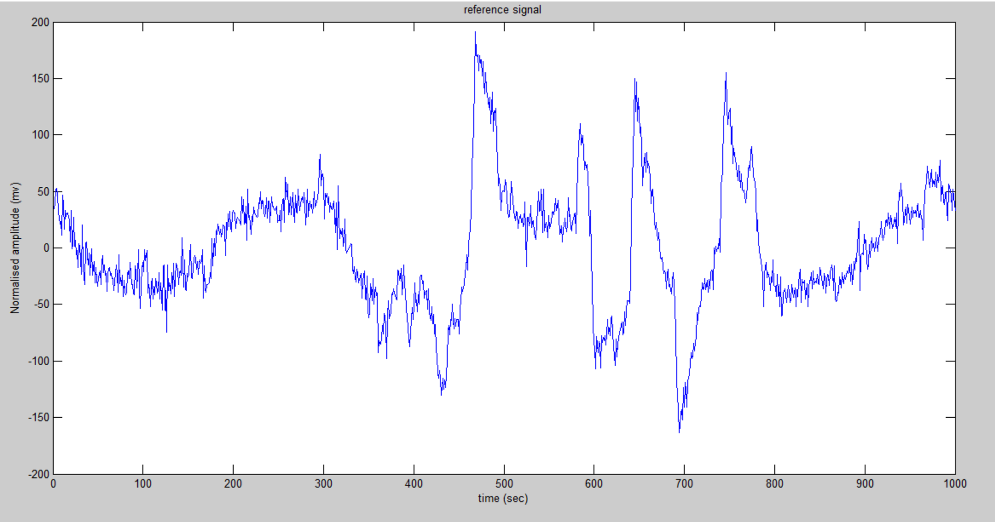

Fig4:reference signal

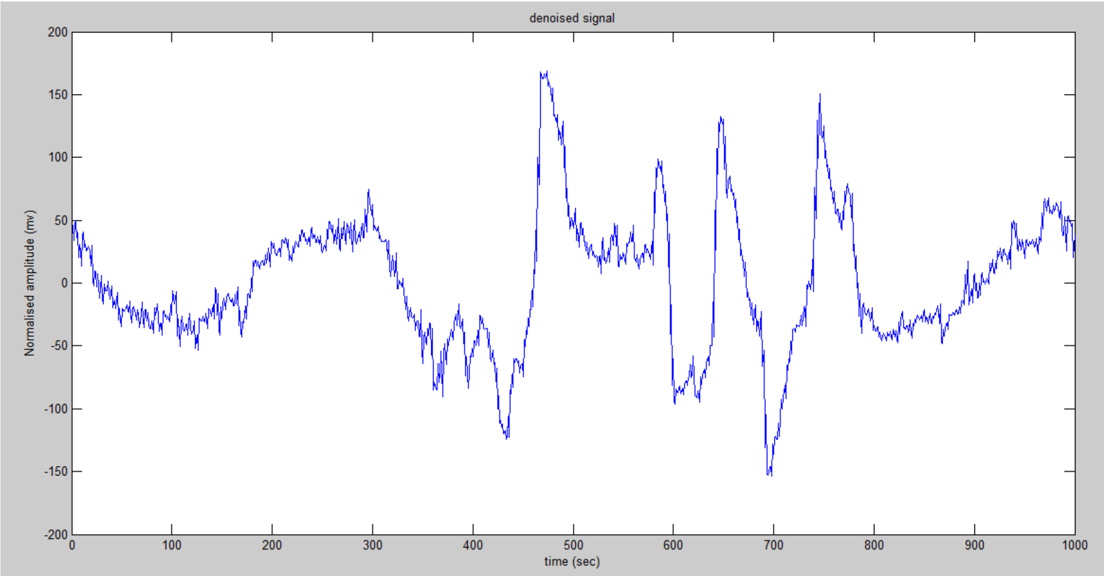

Fig5:Denoised signal

VIII. CONCLUSIONS

An modified daubechies architecture is implemented using MATLAB. The noisy EOG signal is decomposed with DWT which is implemented using modified daubechies architecture. The mean square error, root mean square error and signal to noise ratio values are computed. The high signal to noise ratio of 31.1630 dB and low mean square error of 0.0456 are obtained using the implemented architecture.

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