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ANALYSIS OF 64-BIT 6T, 7T & 8T SRAM CELL – 90 and 180NM TECHNOLOGY

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ABSTRACT

With ever raising demands of battery operated portable device in market has encouraged the VLSI makers to reduce the power dissipation of the electronics devices to increase the battery backup. Static Random Access Memory (Static RAM or SRAM) typically occupies the largest portion of the total digital circuit. The demand for static random-access memory (SRAM) is increasing with large use of SRAM in System On-Chip and high-performance VLSI circuits. The power consumption and speed of SRAMs are most important topic that provides a solution which describes various designs that minimize the consumption of power. This article is based on the motivation of reduction of the average power consumed in SRAM memory and focuses on the analysis in terms of power dissipation, delay and power delay product of the 6-transistors, 7- Transistors and 8- Transistors SRAM memory cell at 180nm technologies by using the Tanner tool which is having a supply voltage of 1.8 volts. The circuit verification is done on the Tanner tool, Schematic of the SRAM cell is designed on the S- Edit and net list simulation done by using T-spice and waveforms are analyzed through the W-edit.

Key Words: CMOS Logic, Low power, Speed, SRAM and VLSI.

I INTRODUCTION

The SRAM is the most commonly used block in Digital Signal Processing (DSP) and its performance and power optimization is of utmost importance for storing the data. With the technology scaling to deep sub-micron, the speed of the circuit increases rapidly. At the same time, the power consumption per chip also increases significantly due to the increasing density of the chip. Hence, in realizing modern Very Large Scale Integration (VLSI) circuits, low-power and high-speed are the two predominant factors which need to be considered. Like any other circuits' design, the design of high-performance and low-power SRAM can be addressed at different levels, such as

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architecture, logic style, layout, and the process technology. As the result, there always exists a trade-off between the design parameters such as speed, power consumption, and area.

Arithmetic circuits, like SRAM, adders and multipliers, are one of the basic components in the design of communication circuits. Recently, an overwhelming interest has been seen in the problems of designing digital systems for communication systems and digital signal processing with low power at no performance penalty. Designing low power high-speed SRAM circuits requires a combination of techniques at four levels; algorithm, architecture, circuit and system levels. They are fast, reliable and efficient components that are utilized to implement any operation. Depending upon the arrangement of the components, there are different types of SRAM available. Particular SRAM architecture is chosen based on the application. The power dissipation in a SRAM is a very important issue as it reflects the total power dissipated by the circuit and hence affects the performance of the device.

Very Large Scale Integration (VLSI) includes wadding large number of electronics devices into lesser areas. VLSI is the process of integrating or merging hundreds of thousands of transistors on a single silicon semiconductor microchip. VLSI technology was considered in the late 1970s when advanced level computer processor microchips were under development.

II BASIC ARCHITECTURE AND WORKING OF SRAM

Figure shows the write mode of conventional SRAM cell. Word line is used for enabling the access transistors M1 and

M2 for write operation. BL and $\overline{BL}$ lines are used to store the data and its compliment. For write operation one BL is High and the other bit line on low condition.

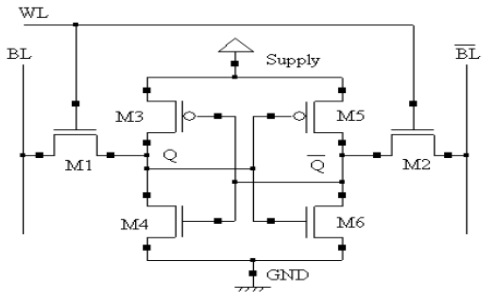

Figure1.1 Conventional 6T SRAM Cell [1]

For writing "0" BL is Low and $\overline{BL}$ is high. When we assert the word line high transistor M1 and M4 is on and any charged stored in the BL goes through M1- M4 path to ground. Due to Zero value at Q the M5 transistor is ON and M6 is OFF so the charged stored at Q. bar line. Similarly in the write "1" operation BL is high due to this M6 is ON

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and the charge store on is discharged through the M2-M6 path and due to this low value on the M3 is ON and M4 is OFF so the charged stored on the Q.

Memory Architecture is Random-access architecture which is an Asynchronous design. The name is derived from the fact that memory locations (addresses) can be accessed in random order at a fixed rate, independent of physical location, for reading or writing. The storage array, or core, is made up of simple cell circuits arranged to share connections in horizontal rows and vertical columns. The horizontal lines, which are driven only from outside the storage array, are called word

lines, while the vertical lines, along which data flow into and out of cells, are called bit lines. A cell is accessed for reading or writing by selecting its row and column. Each Cell can store 0 or 1. Memories may simultaneously select 4, 8, 16, 32, or 64 columns in one row depending on the application. The row and column (or groups of columns) to be selected are determined by decoding binary address information. For example, consider a row decoder that has 2 n out-put lines, a different one of which is enabled for each different n-bit input code. The column decoder takes m inputs and produces 2 m bit line access signals, of which any of them can be enabled at one time. The bit selection is done using a multiplexer circuit to direct the corresponding cell outputs to data registers. In total, 2 n X 2 m cells are stored in the core array. In this design, the number of rows and columns, both are equal to 64 for 4Mb memory cut. Using two such memory cuts, a 8Mb SRAM memory is designed. The SRAM IC is R/W memory circuit that permits the modification (writing) of data bits to be stored in a memory array, as well as their retrieval (reading). The SRAM IC was developed using the CDS IC446, cadence IC design environment. The design was based on the AMI 0.6-micron process. The SRAM IC design consists of SRAM cells, pre charge, sense amplifiers, mux, nand gates, and gates, nor gates and row decoder. The most important part is the cell as all the other circuitry is connected to and around the cell. The popular, full CMOS 6-transistor cell configuration was used to design the SRAM memory array [2]. Some of the advantages of using full CMOS SRAM configuration are low static power dissipation, superior noise margins, high switching speeds and suitability for high-density SRAM arrays. In order to design a 64 bit SRAM, 64 full CMOS 6-T cells were used. Each full CMOS 6-T cell has a capability of storing 1 bit [10].

As per the Literature review we have concluded that there is lot of work done for the reduction of dynamic power dissipation and also there are research paper which is targeting the static power dissipation. As the technology goes down the power dissipation becomes the main design criteria in SRAM memory design. Because memory will decides the total power dissipation. Based on the above literature survey and after carefully analyzing the previous work we have optimized the short circuit power dissipation in SRAM memory cell. Based on the literature survey we have concluded that SRAM memory cell dissipate large amount of short circuit power during rise time and fall time of input data because at that time the direct path exist between the V_{dd} and ground in a single cell the short

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circuit power is micro watt range at 90 nm technology as the size of memory increases the amount of power increases corresponding .so based on the previous work we have decided to optimize the short circuit power.

Static random access memory (SRAM), the most widely used embedded memory, typically occupies the largest portion of SoC die area, and often dominates the total chip power. In order to maintain performance, however, this has required a corresponding reduction in the transistor oxide thickness to provide sufficient current drive at the reduced supply voltages. To further reduce the leakage current, the stacking effect is used by switching off the stack transistors when the memory is ideal**.** The transistors have been lowered which also contributes to leakage currents and reduces the battery life dramatically. The low power reduction techniques reduce the leakage based on the dependencies of the tunneling currents on the terminal voltages, the gate oxide thickness, and the type of the transistor. Various efficient techniques which gives overall best performance over existing SRAM design approaches that allow the analysis and simulations of different parameters at 90nm and 45nm technology successfully on the basis of the power dissipation, speed and their temperature dependence with the area efficiency of the circuit.

1. **Power Consumption in CMOS Circuits**

There are three main components of power consumption in digital CMOS VLSI circuits.

a. **Switching Power**: consumed in charging and discharging of the circuit capacitances during transistor switching.

b. **Short-Circuit Power**: consumed due to short-circuit current flowing from power supply to ground during transistor switching. This power more dominates in Deep Sub Micron (DSM) technology.

c. **Static Power**: consumed due to static and leakage currents flowing while the circuit is in a stable state. The first two components are referred to as dynamic power, since power is consumed dynamically while the circuit is changing states. Dynamic power accounts for the majority of the total power consumption in digital CMOS VLSI circuits at micron technology [15], [16].

$$P_{avg}=P_{Switching}+P_{Short\text{-}Circuit}+P_{Leakage}$$

$$=(\alpha_{0\rightarrow 1}\times C_L\times V_{dd}^{2}\times f_{clk})+(I_{sc}\times V_{dd})+(I_{leakage}\times V_{dd})$$

III SCHEMATIC OF LOW POWER SRAM CELL

Below Figures are of 1 Bit SRAM Cell using 6T, 7T & 8T shows the write mode of low power SRAM cell. Word line is used for enabling the access transistors M1 and M2 for write operation. BL and $\overline{BL}$ lines are used to store the data and its compliment. For write operation one BL is High and the other bit line on low condition. In low power SRAM cell we introduced one Control signal transistor for controlling these transistors. But due to one more

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transistors area for low power SRAM cell is increased in comparison to Conventional approach. This control transistor uses control select signals which can be properly control the short circuit power dissipation. During write operation this transistor which has control signal works as in on condition. During read operation it will remain in off condition. When this transistor is in off condition will break the path which is in between V_{dd} and Ground.

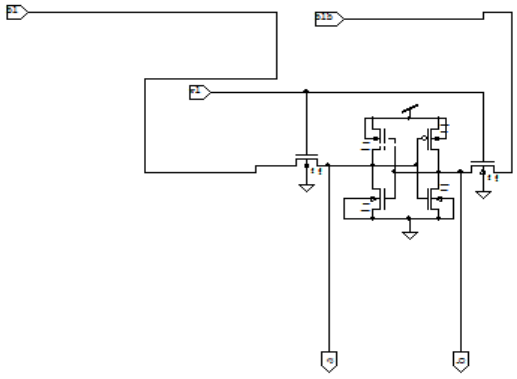

Figure 3.1 6-T SRAM cell

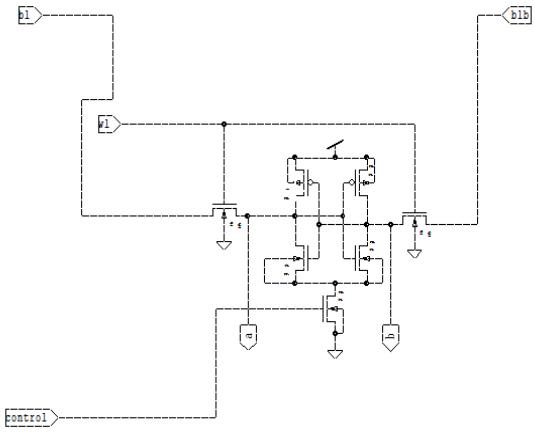

Figure 3.2 7-T SRAM cell

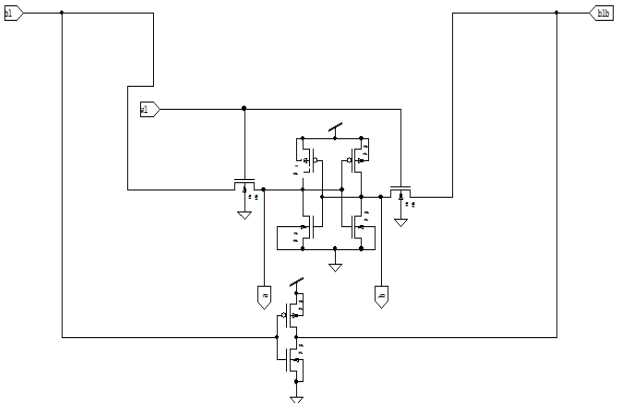

Figure 3.3 8-T SRAM cell

IV FINAL RESULT

In above show the output waveforms of 1-bit 6T SRAM cell. The output waveforms of all circuits look like same. But power and delay are the difference between them as shown in below table

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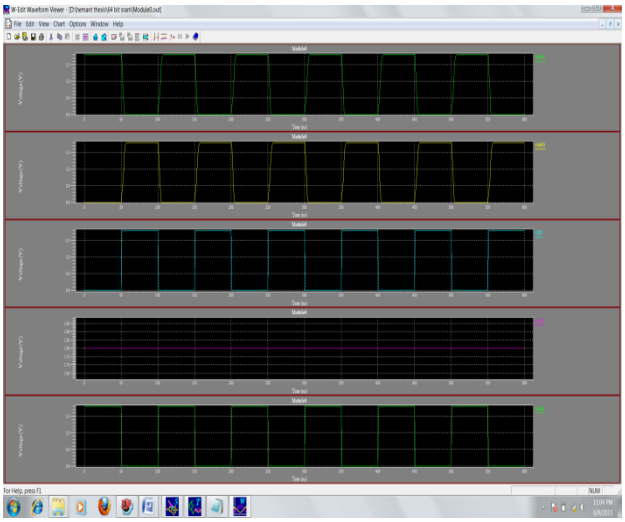

Output waveforms of 64-bits SRAM cell

Performance parameters of 64 Bit Different SRAM Cell

Design Style	No.of Transistors	Min Length (nm)	Avg. Power Cons. (watts)	Prop. Delay (sec)	Power Delay Product
6-T	384	180	8.48×10^{-3}	9.12×10^{-12}	77.33×10^{-15}
7-T	448	180	2.16×10^{-4}	2.70×10^{-9}	5.83×10^{-13}
8-T	512	180	7.93×10^{-3}	2.94×10^{-9}	23.32×10^{-12}

V CONCLUSION

The design and implementation of the SRAM memory is shown in this paper. In this paper we design 6T, 7T & 8T SRAM memory cell. The total power consumption is also significantly lower as compared to the existing papers based on SRAM. So according to the requirement we can use these SRAM memory cells can be used in internal CPU. The low power operation is achieved without sacrificing performance of memory. Power consumption is a function of load capacitance, frequency of operation, and supply voltage. A reduction of any one of these is beneficial. A reduction in power consumption provides several benefits. Less heat is generated, which reduces problems associated with high temperature, such as the need for heat sinks. This provides the consumer with a product that costs less. Furthermore, the reliability of the system is increased due to lower-temperature stress gradients on the device. An additional benefit of the reduced power consumption is the extended life of the battery

in battery-powered systems. In this paper we concluded that power dissipation and delay are less than the base paper.

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