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A REVIEW ON QUANTUM DOT CELLULAR AUTOMATA

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ABSTRACT

The scaling of CMOS effect the performance of digital circuits due to factors like heat dissipation and power consumption. The various limitations of CMOS such as heat dissipation, power consumption, size etc. can be overcome by quantum dot cellular automata (QCA). QCA is an efficient technology that provides smaller size, faster response, low power consumption. QCA provides the new and efficient method of computation and information transformation. The main focus of this paper is to study the trends which are proposed to design various digital circuits.

Keywords: Majority Gate (MV), QCA

I. INTRODUCTION

The priorities of digital industry have been changed in the few past years due to technology advancement. Conventional CMOS and BJT based devices satisfies the shrinkage of the size of transistors according to Moore's law. However, scaling down of transistors using traditional technologies offers threats to some of the critical features of the digital devices. Due to the coulomb interactions, QCA is an alternative approach to CMOS transistor based devices. QCA provides ultra low power consumption and high clock rate (order of tera-hertz).

In 1993, QCA was proposed by C. S. Lent et al. [12] from the University of Notre Dame. A Quantum dot Cellular Automata is a nanostructure of square shape which is able to perform computational functions. In contrast to traditional computers, QCA technology transfers information through the polarization state of various cells instead of channeling information through current and voltage. QCA provides high switching speed, high device density and low power consumption. In 1997, QCA cell was fabricated for the first time. In QCA, both combinational and sequential circuits can be implemented [13].

The basic structure is the QCA cell that has four quantum dots at the corners of the square shaped structure and two electrons. The two electrons can occupy any of the two quantum dots. The two electrons can tunnel between quantum dots but cannot come out from the cell because of high potential barrier. Due to the coulomb interactions, the electron can be located at opposite ends of a diagonal. A single electron has two states called Polarizations i.e. P=+1 and P=-1. The P=+1 state represents the logic 1 and P=-1 represents the logic 0. The cell polarization is defined in equation 1.

$$P = \frac{(\rho 2+\rho 4)-(\rho 1+\rho 3)}{(\rho 1+\rho 2+\rho 3+\rho 4)} \quad (1)$$

where ρ_I is the electronic charge at dot i.

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When two quantum cells are placed near each other, the polarization gets affected. When we place many quantum cells together, they form a wire and the polarization of second cell will be affected by the polarization of first cell. Consider the first cell to be having polarization P=+1 then the second cell placed nearer will be having same polarization P=+1 to minimize coulomb interactions. Following is the basic quantum cell and quantum wire diagram.

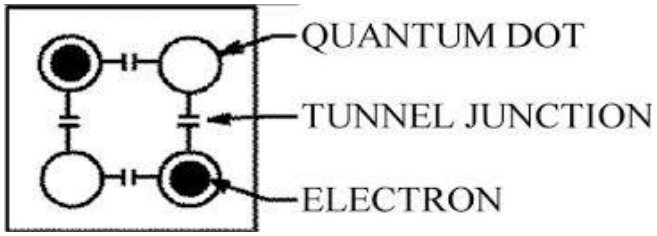

Fig1a. Quantum Cell [2]

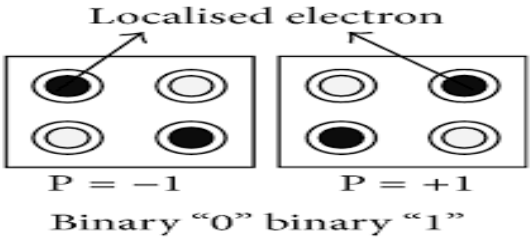

Fig1b.Polarizations of QCA cell [2]

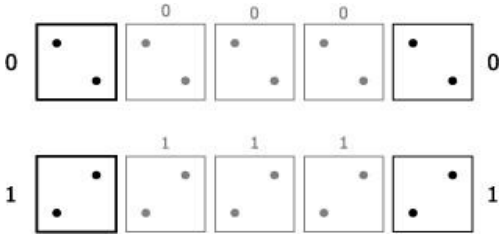

Fig1c. Quantum cell wires [2]

The majority gate (fig.2) is the most important basic QCA logic device because it is used to build AND and OR gates, besides being used to builds more complex devices. The central cell of the gate has lowest energy and it assumes the polarization of majority of the three input cells as it is the stage where the repulsion between the electrons in the here input cells and electron in the device cell is smallest. If the input cell C has polarization representing binary 0, the output cell has same polarization of A and B which are majority in this case. If the cell C is fixed at binary 0 then AND gate with the two inputs A and B is defined. Similarly if the input C is fixed at binary 1 then the OR gate with the inputs A and B is defined. So, any computational circuit can be fulfilled with QCA.

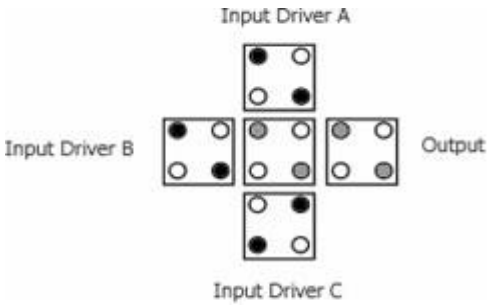

Fig 2 A QCA majority gate [7]

QCA CLOCKING

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Clock in QCA is not only to synchronize and control information flow but actually provides power to run the circuit. QCA cell is clocked using a four-phase clocking scheme shown in Fig.1.9. Signal strength is restored by changing clock phase. The four phases correspond to switch, hold, release, and relax; the lag between adjacent phase is 90°. In switch phase cells being unpolarised with low potential barriers but the barriers are raised during this phase. In hold phase barrier are held high while in release phase the barrier are lowered. In relax phase, the barriers remain lowered and cells in unpolarised.

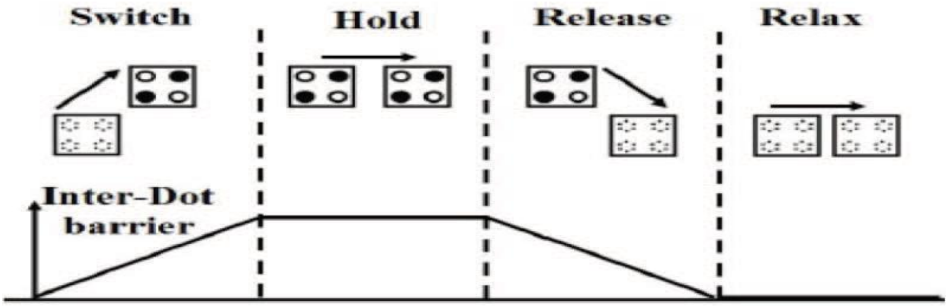

Figure 3 Clocking Schemes [13]

II. LITERATURE SURVEY

In 2010, Pijush Kanti Bhattacharjee et al. [1], proposed the design of adder both half adder and full adder using AND-NAND (A-NA) and OR-NOR (O-NO) gates designed by QCA and compared it with conventional gates like AND, OR, EX-OR, CMOS gates. The adder circuit design is easy to realize practically with minimum no. of gates using QCA technology especially with A-NA and O-NO gates. In all aspects, QCA based adder circuit design is an excellent tool in forthcoming generation having different combinational circuits.

In 2010, Pijush Kanti Bhattacharjee et al. [2], proposed the design of symmetric functions by using QCA gates which is practically to realize with lesser no. of gates. The method used is classical logic, where its uses 2-inputs and 2-outputs AND-NAND and OR-NOR cells designed by QCA. The symmetric function consists of different Boolean functions with the adder circuit functions and all other combinational circuits like subtractor, multiplier, divisor, multiplexer, encoder etc. can be designed, providing reduction in hardware cost as well as delay relative to other techniques present.

In 2012, Mostafa Abdollahian Dehkordi et al. [3], proposed a new design of D-flip flop using QCA technology which reduces the number of cells used to build D-flip flop.

In 2013, Bibhash sen et al. [4], developed sequential circuits in QCA under multilayer framework to achieve minimum delay in logic realization. The proposed multilayer design has improvement in device density and delay. The design offers 100 % fault tolerance under cell deposition defect.

In 2013, J.Iqbal et al. [5], proposed the design of modular MUX-DEMUX in QCA. The proposed design achieves significant improvement in terms of area, speed, complexity over the traditional approaches. The simulation results provide less complexity to the reported designs.

In 2014, Mrinal Goswami et al. [6], proposed the implementation of EX-OR, EX-NOR logic gates and arithmetic logic units using QCA multiplexers. Sequential circuits are also designed using QCA multiplexer. The proposed design provides improvement in device density, cell count and clock delay as compared to previous designs.

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In 2014, Ali Newaz Bahar et al. [7], proposed that quantum dot cellular automata is the emerging technology for designing low power consuming logic devices. The no. of cells required, area which they are covering, the clock used and the delay of the reversible gates is much less than a CMOS. Also the power consumption is low and operating frequency is high.

In 2014, M.Prabakaran et al. [8], proposed the design for QCA full adder, full subtractor, ring counter, T flip flop. This layout is done by using QCA designer and the design is analyzed using majority gates and invertors. Simulations show that the occupied area is 0.25m for this particular design.

In 2015, Nitesh Gupta et al. [9], gave the design for novel gate for realization of QCA based logic designs. A new AIN gate is designed using which we can design various combinational circuits. The proposed AIN gate achieves improvement in terms of cell count, response time and size.

In 2015, Mrs. Libi Balakrishnan et al. [10], proposed the effective design of logic gates and circuits using QCA. The proposed designs can be used for designing complex circuits as these are utilizing minimum number of QCA cells with no cross overs. The proposed design provides less QCA cells complexity, lesser clock delays and reduced area.

In 2016, Mahalakshmi KS et al. in 2016 [11], gave performance estimation of conventional and reversible logic circuits and sequential circuits using QCA technique. Few combinational circuits and sequential circuits such as counters and registers are designed using different topologies of QCA. The results are compared with reverse logic gates which conclude that reverse logic combinational circuit implementation consumes more area and energy.

III.IMPLEMENTATION

QCA (quantum cellular automata) designer is the simulator which is used to design any combinational and sequential circuit and then simulate the designed circuit. In QCA Designer we can design the required circuit using cells or arrays, rotate them, copy the structure for multiple use and provide clocks tom it to make it work at different time interval. Hence QCA designer is an effective tool to design any combinational and sequential circuit. Following are some gates designed in QCA designer.

AND and OR GATE Design

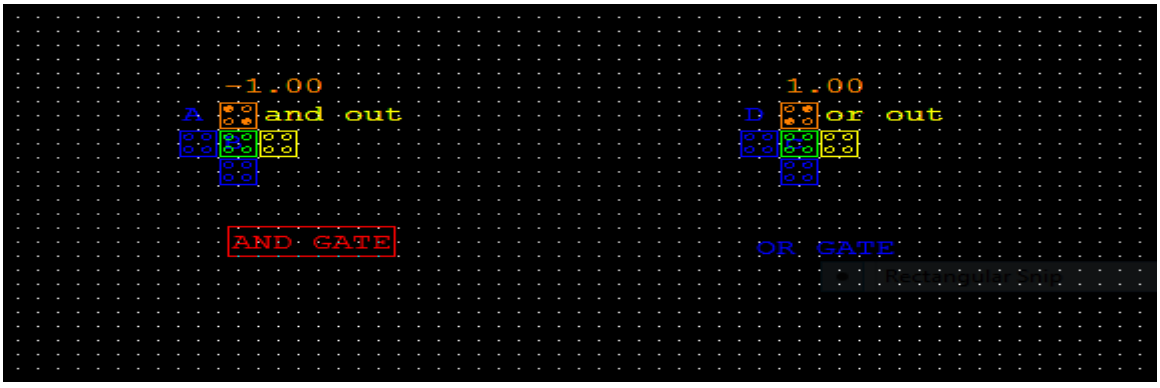

Figure4a. Design of AND or Gate

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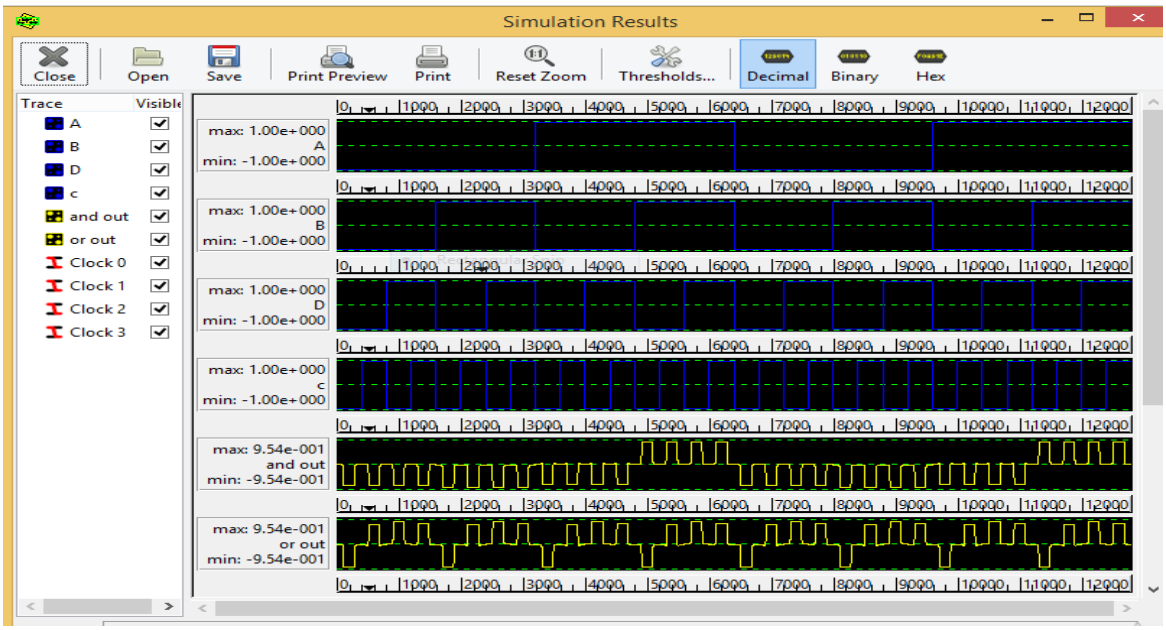

Figure 4b Simulation Result of AND and OR gates

INVERTOR DESIGN

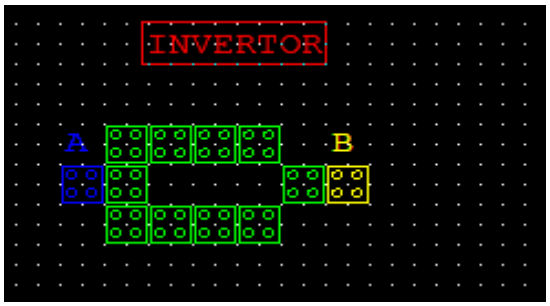

Figure 5a Invertor Design

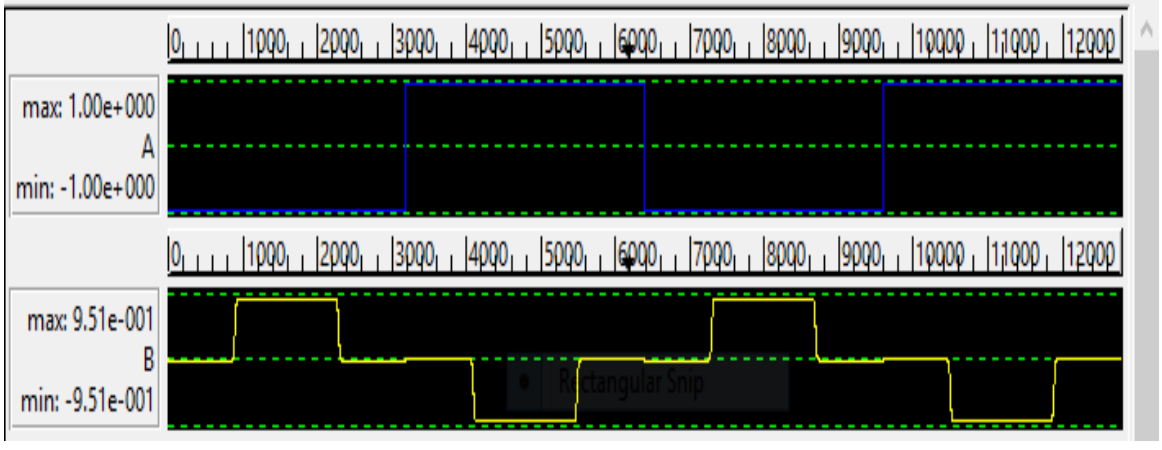

Figure 5b Simulation result of invertor

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NAND and NOR gate

Figure 6a NAND and NOR gate design

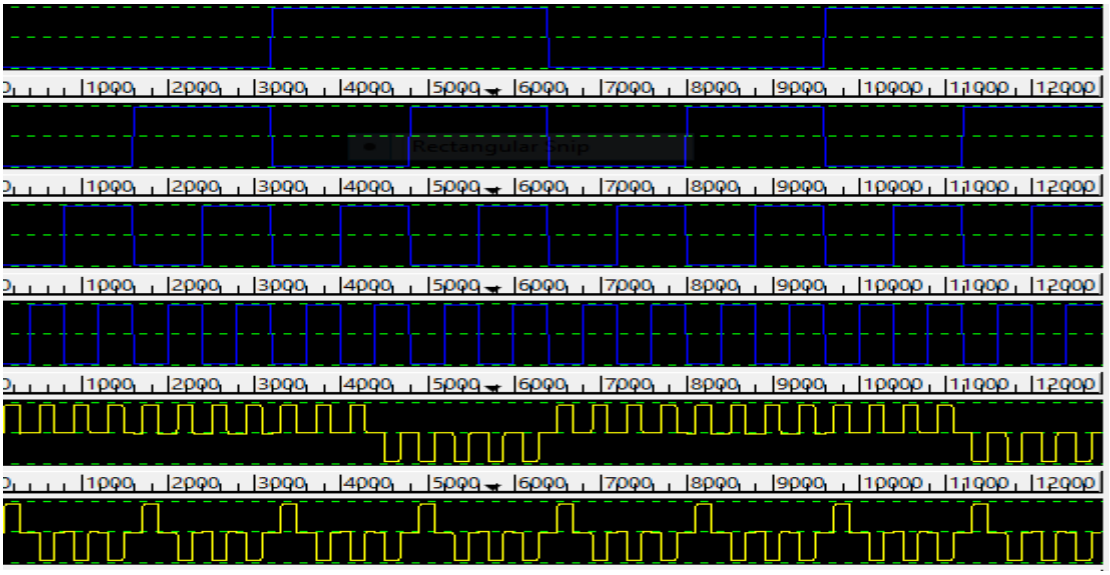
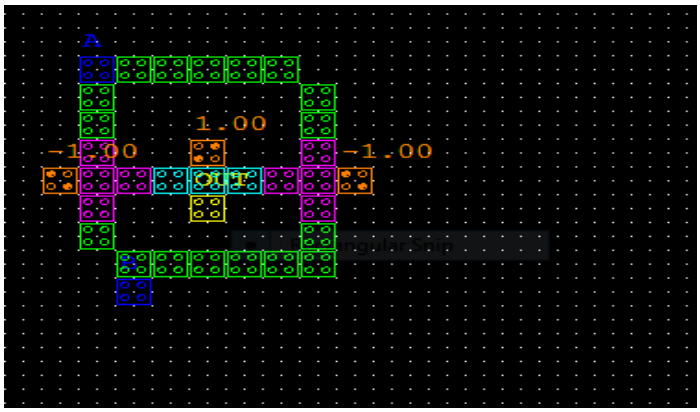


Figure 6b Simulation Result of NAND and NOR gate

EXOR gate and EXNOR gate design



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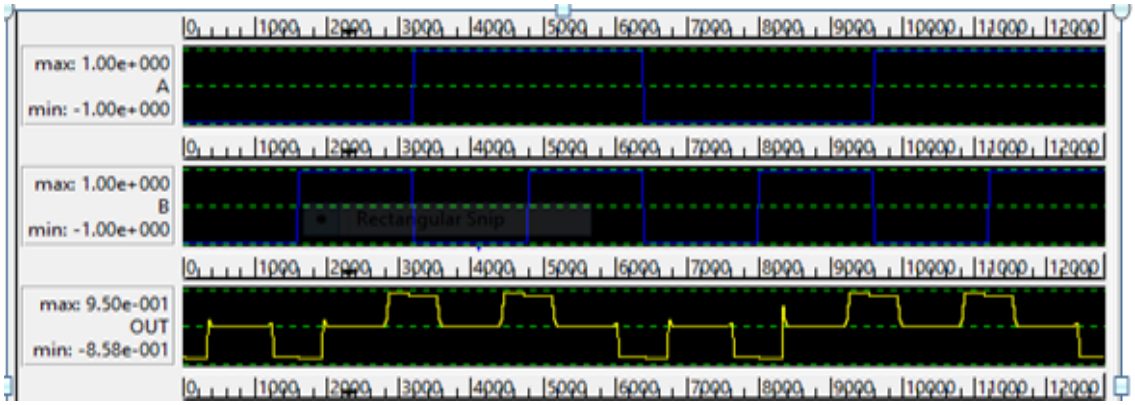

Figure 7b Simulation Result of EXOR gate

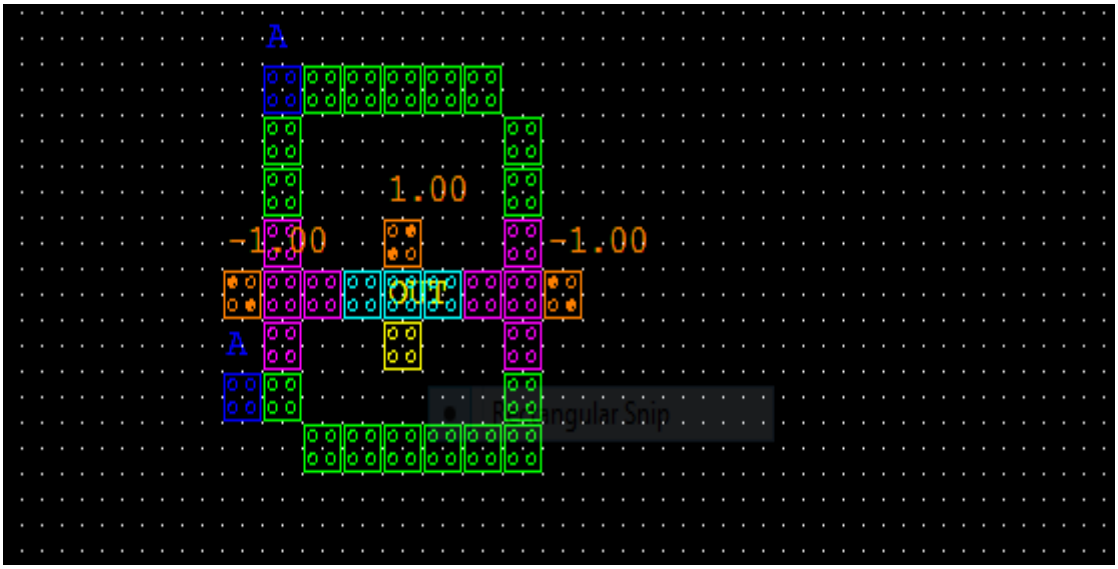

Figure 8a EXNOR design

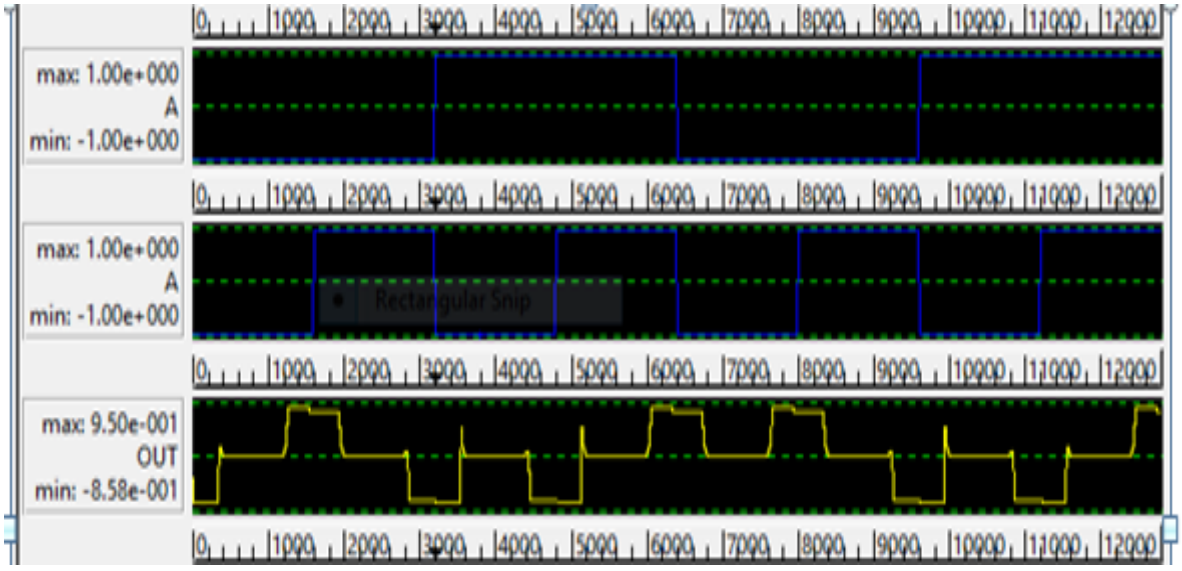

Figure 8b Simulation Result of EXNOR Gate

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HALF ADDER

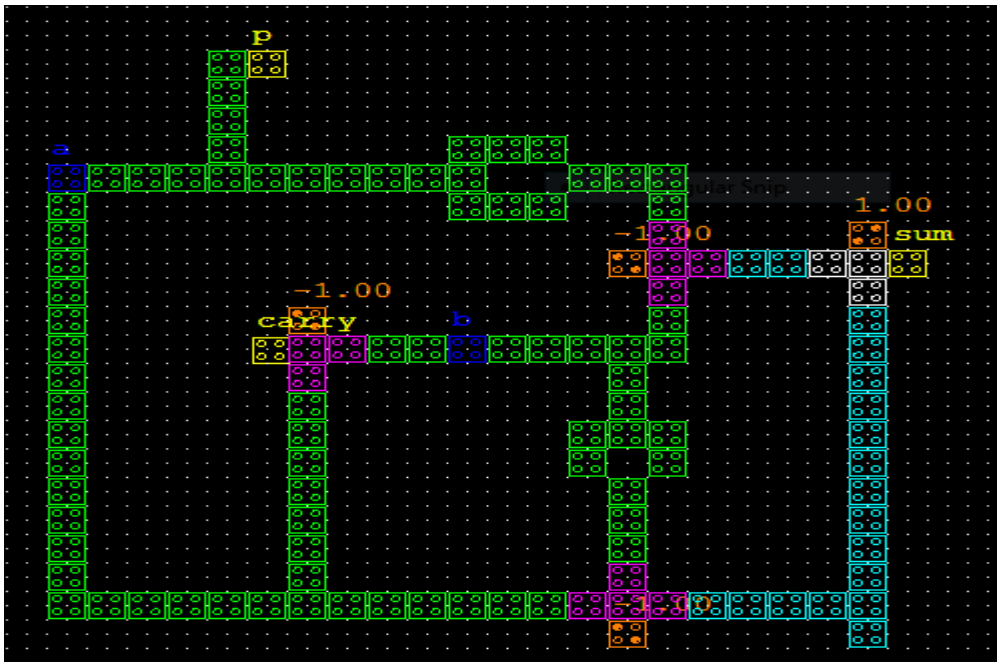

Figure 9a Design of HALF ADDER

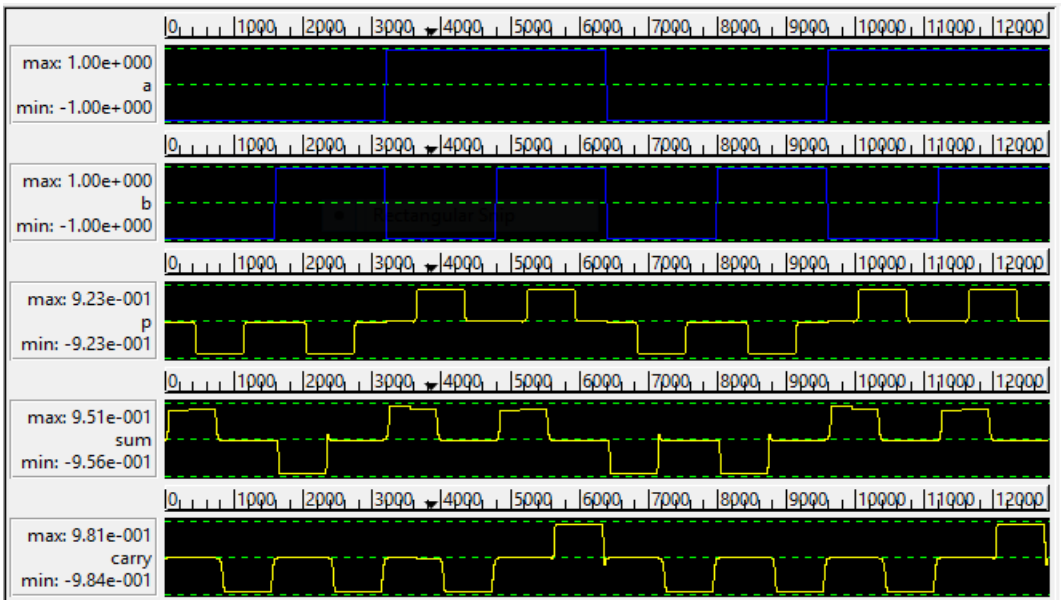

Figure 9b Simulation Result of HALF ADDER

IV. CONCLUSION

Quantum Cellular Automata is a new technology developing to create quantum computing devices. In this paper we have discussed several aspects of QCA technique with their working approach and enhancements. These designs provide better results as compared to the CMOS technology in terms of small area, high speed, high frequency, low power computation, fault tolerance. We discussed the design of various digital circuits like half adder, full adder, mux, de-mux, subtractor, flip flops.

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