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DESIGN OF 3:8 REVERSIBLE DECODER USING R-GATE

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ABSTRACT

The area of reversible logic has received great importance in the recent years because of its beneficial feature of reduction in power dissipation. Massive research is currently been undertaken on sequential and combinational circuits using reversible logic. Decoders are one of the most important circuits used in combinational logic. In microprocessor/microcontroller-based systems, the most commonly used block is the instruction set decoder. However, instruction set decoders consumes large amounts of power. Thus optimizing the power of this block could aid in reducing the overall power consumption of the system. Different approaches have been proposed for designing a tightly constraints compact algorithm. In this paper, an approach for designing is carried on a novel design of 2:4 decoders and has been used it to build a 3:8 decoder. The performance metrics of decoder has been compared with a previously existing design and mathematical estimation of the quantum cost for n inputs decoder has been provided.

Keywords: Reversible Logic, Garbage Outputs, Quantum Cost, Delay, Reversible Decoder, Constant Inputs

I. INTRODUCTION

In Very Large Scale Integrated Circuits (VLSI) designs today, the device dimensions are shrinking exponentially and so the circuit complexity is growing exponentially. Further, device scaling is limited by the power dissipation; demanding for better power optimizations methods.

According to Rolf Landauer [1], heat generated due to the loss of one bit of information during computation is about KTln2 in joules where K is the Boltzmann constant and T is the absolute temperature at which computation is performed. At room temperature loss of one bit of information generate small amount of heat, but when number of bit is more as in case of high speed computation work, the heat dissipated by then will be so large that it can affect the performance and result in reduction of lifetime of circuits. Since in reversible circuits number of bit loss is there hence ideally in reversible circuits no power dissipation occurs. But practically some power dissipation do occur, which is much less than the conventional logic.

C.H. Bennett [2], observed that dissipated energy is directly proportional to the number of bit lost. Bennett later showed that this heat dissipation could be avoided by using reversible computation. We can avoid KTln2 joules of energy dissipation by constructing circuit using reversible logic gate, this is because reversible bit does not require any bit of information. This proof by Bennett has led to an extensive research on reversible logic. In today's computing era, the need of reversible computing cannot be ignored. Reversible computation can be

performed in a system only when the system comprises of reversible circuits**.** A quantum computer will be viewed as a quantum network (or a family of quantum networks) composed of quantum logic gates; It has applications in various research areas such as Low Power Complementary Metal Oxide Semiconductor (CMOS) design, quantum computing, nanotecnology, DNA Computing.

Reversible circuits are those circuits, which have one-to-one mapping between input and output vectors. A circuit/gate is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one-to-one correspondence in order to preserve information during computation.

The paper has been arranged in the following manner. Section 1 includes the introduction of reversibility. Section 2 describes the basic definitions, basic concept and various reversible logic gates. An efficient approach towards designing of 3-to-8 reversible decoders is shown in section 3. Section 4 shows the work done by various researchers in the field of reversibility. Section 5 includes the Analysis and Scope of work and later Section 6 includes Conclusion. References are shown next.

II. BASIC DEFINITIONS AND CONCEPTS

In his section, we have presented the basic ideas on performance parameters which determining the complexity and performance of circuits and some popular reversible gates. The main purposes of designing reversible logic are to decrease quantum cost, depth of the circuits, the number of garbage outputs, constant inputs, area and power. Reduction of these parameters is the bulk of the work involved in designing a reversible circuit.

2.1 Quantum Cost

The total number of basic quantum gates in the circuit is known as quantum cost of that circuit Qunatum cost of a reversible. Quantum cost of all 1x1 and 2x2 reversible gates are unity.

2.2 Garbage Output

In a reversible quantum circuit, there are some unused or unwanted outputs, which are not further required. They are only used to maintain the reversibility of device.

2.3 Constant Input

This refers to the number of inputs that are to be maintained constants at either 0 or 1 in order to synthesize the given logical function.

2.4 Area and Power

Area of a gate is defined by the feature size. As the basic quantum gates are fabricated with quantum dots with the size ranges [1], [2] from several to tens of nanometers (10^{-9} m) in diameter, the size of the basic quantum gates ranges from 50 Angstrom - 300 Angstrom [1], [2]. The area of a gate can be defined as follows:

Area = Number of Quantum Gates X Size of Basic Quantum Gates . . . . (1)

Power of a gate is defined by the energy. Energy of basic quantum gates is 142.3 meV [1], [2]. So, the power of a gate can be defined as follows:

Power = Number of Quantum Gates X Energy of Basic Quantum Gates . . . . (2).

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2.5 Delay

In our delay calculations, we use the logical depth as the measure of the delay [3]. The delay of a quantum gate can be computed by calculating its logical depth when it is designed from smaller 1x1 and 2x2 quantum gates. The delay of a circuit is the delay of the critical path. The path with maximum number of gates from any input to any output is the critical path [4].

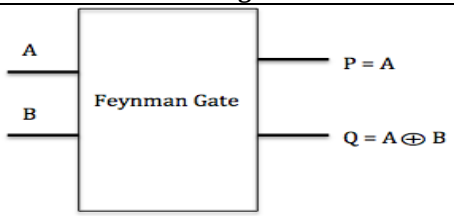
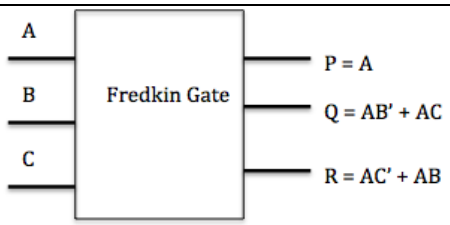
2.6 Fault Tolerant Gates

A Fault tolerant gate is a reversible gate that constantly preserves same parity between input and output vectors, which allows detecting a faulty signal from the circuit's primary output. Researchers [5, 6] have showed that the circuit consist of only reversible fault tolerant gates Feynman Double Gate and Fredkin Gate a F2G preserves parity and thus able to detect the faulty signal at its primary output. An important advantage of the technique is that the logic design of a reversible circuit remains the same and the reversible circuit need not be redesigned for adding the testability feature to it.

2.7 Reversible Gates

The few reversible logic gates have been presented in TABLE 1. These gates are used in designing of more complex system having reversible circuits as a primitive component and which can execute more complicated operations using quantum computers. In a reversible logic gate there is always a unique input associated with a unique output and vice versa. Researchers have developed several primitive reversible gates, including the Feynman, Toffoli, Fredkin, and Peres gates [7] and many more. Basic Quantum gates are Controlled-V, controlled-V^{+}, CNOT Gate and NOT Gate. Some basic reversible gates are introduced in this section.

Table-1: Reversible Gates with description and their block diagram

Reversible Gate	Description	Block Digram
Feynman Gate	The Feynman Gate (FG) or Controlled Gate may be a 2-inputs and 2-outputs reversible gate with the mapping (A, B) to (P, Q) with quantum cost value 1	 **Figure 1: Feynman Gate**
Fredkin Gate	The Fredkin Gate (FRG) is a 3x3 reversible logic gate with 3-inputs and 3-outputs with the mapping (A, B, C) to (P, Q, R). Fredkin gate quantum cost is 5	 **Figure 2: Fredkin Gate**

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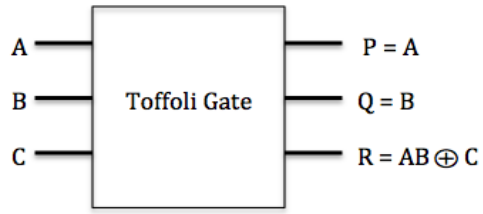
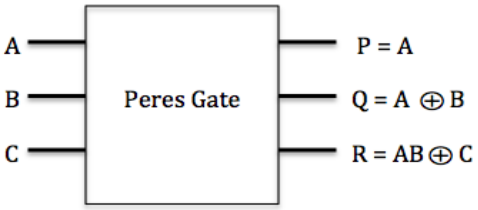
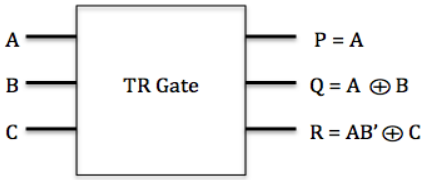
Toffoli Gate	The Toffoli Gate (TG) is a 3x3 reversible gate with quantum cost 5. Toffoli gate is having 3 inputs and 3 outputs, which maps (A, B, C) to (P, Q, R).	 **Figure 3: Toffoli Gate**
Peres Gate	The Peres Gate is 3X3 reversible gate with a mapping between the inputs and the outputs as (A, B, C) to (P, Q, R, S) having quantum cost 4.	 **Figure 4: Peres Gate**
TR Gate	TR Gate is a 3x3 revrsible gate with quantum cost as 4.	 **Figure 5: TR Gate**

III. PROPOSED REVERSIBLE DECODER

Hardware of digital communication systems relies heavily on decoders as it retrieves information from coded output. Fig. 6 shows the block diagram of 2:4 decoder, which can take the form of a multiple-input, multiple-output logic circuit that converts coded inputs into coded outputs, where the input and output codes are different. The proposed 2-to-4 reversible decoder requires only one gate without any garbage output which has 7 quantum cost. Our proposed design has the same gate count, garbage outputs and delay. But it has improved quantum cost. A reversible 3-to-8 decoder can be designed using one 2-to-4 reversible decoder and four R gates. R is a 3x3 reversible gate having inputs (A, B, C) and outputs P = A; Q = AB and R = A'B + AC. The achievement of the design of 3-to-8 reversible decoder designs was greater as the existing best in terms of quantum cost and delay. Quantum cost of 3-to-8 reversible decoder using R gate is 23 when compared by using FRG Gate which is about 27. Fig. 7 shows diagram of 3-to-8 decoder using HL [8] and R Gates.

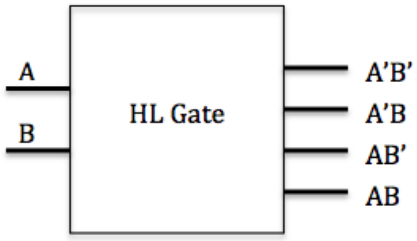


Figure 6: 2-To-4 Decoder

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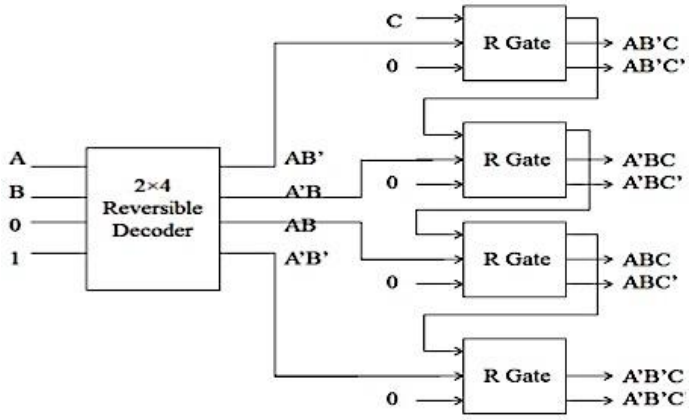

Figure7: efficient approach for 3-to-8 decoder using HL gate and R gate.

IV. CRITICAL LITERATURE REVIEW

The review was based on a selection of published literature predominantly. The time frame is 2006 -2016. The search is related to relavant published papers on reversible decoder within a time frame and it has been observed that there is scope of further work. In this paper revresible decoder design is proposed using R gate and design is compared with the exsiting counterpart in terms of performance analysis. Research papers which discussed on n-to-2^n reversible decoder using reversible logic are shortlisted for work.

The internal architecture of CPU consisting of Control Unit, ALU, Register files and various components which plays an important role in performance of whole CPU. Control Unit directs the operation within the computer processor by directing the inputs and outputs of computer system. Important block of control unit is decoder, which is used to control the memory components of processor plays an extensively important role in performance of overall CPU. Hence it will be not wrong if we say the instruction set decoder consumes more power. Thus optimizing the power of this block will be helpful to reduce the overall power consumption of the system. According to this survey the researchers have already proposed reversible designs of many common arithmetic and logical units, including adders, multipliers, shifters and even registers and other reversible component. Very little focused work has been done specifically on reversible decoder design. A Decoder is a fundamental building block in many computing systems. To design decoder at first we propose a reversible 2-to-4 decoder, which was used to construct a 3-to-8 decoder and so on.

A 2-to-4 decoder must generate the four logical AND functions A'B', A'B, AB', AB. In [9] a reversible 2-to-4 decoder was designed by using four independent reversible two-input AND gates. But this design incurs a quantum cost at least four times the quantum cost of a single reversible AND function does not provide better performance. Nachtigal & Ranganathan in 2011 [10] proposed a 2-to-4 reversible decoder, which generates all four necessary AND functions using a single Fredkin gate and minimal supplementary logic has quantum cost 8, two constant inputs, and zero garbage outputs. The design is not optimized in terms of quantum gates and delay and also didn't show the total required area, power and quantum gate calculation complexity of the circuit. Moreover, the theoretical explanation and algorithm of the design are also absent in this work. Ravish Aradhya

HV, Et al. in year 2012 [11] designs the 2:4 Decoder, which requires 1 Feynman and 2 Fredkin Gates. This design requires a total of 3 gates with constant input 3 and garbage output as 1. This design requires a total of 3 gates, number of inputs is 5, which include 2 variable inputs and 3 constant inputs, garbage output 1, delay of 1 and quantum cost 11. This work in terms of performance is quite effective but the design algorithm has not been extended for further 3:8 and 4:16 decoder. Arvind Kumar, Et al. [12] concluded that the 2 to 4 decoder using three fredkin gates. Since in all three Fredkin gates same number of inputs and outputs resulting in less power dissipation as compared to conventional logic gates. Hence by making use of fredkin gates in similar manner any n to 2^n decoder can be designed. Here n represents the number of inputs. In this paper a 4 to 16 decoder has been designed using proposed 2-to-4 decoder uses 15 constant inputs and four garbage outputs. But with three Fredkin gates, again the total delay is more along with more power consumption. Which is not an effective approach in designing decoder. Md. Shamsujjoha and Hasan Babu proposed a fault tolerant reversible decoder [5, 6] in 2013. Only a F2G can work as 1-to-2 Reversible Fault tolerant Decoder (RFD) can be used in parallel circuits, multiple-symbol differential detection, network components and in digital signal processing etc. A 2-to-4 reversible fault tolerant decoder can be realized with at least 12-quantum cost using one F2G and 2 FRG and further a 3-to-8 reversible fault tolerant decoder design requires six Fredkin gates and one Feynman double gate. The constructed circuit can detect any single bit errors that include single bit stuck-at-fault. An advantage is that the technique ensures that the garbage generated during the process of conversion to testable reversible circuit is minimized.

But the design is not optimized in terms of quantum gates, constant inputs, and delay also didn't show the total required area and power of the circuit. Neeta Pandey, Et al. [13] illustrated that a 2:4 reversible decoder, which can provide active high as well as active low outputs has quantum cost of 12, constant inputs 2 and single garbage output. The decoder uses 2 Feynman and 2 Fredkin gates and has low quantum cost. Design is extended to 3:8 decoder that uses 2:4 decoders and cascade it with Fredkin and Feynman Gates followed by an n-input decoder. It also uses an additional 1 to 5-tracer circuit in order to remove the fan out problem in the reversible decoder. The structure is more efficient than its previous counterparts. But design is not much optimized in terms of overall cost metric, delay and hardware complexity. The cost metrics of the proposed decoder can further be reduced if there is no tracer circuit. Ritajit Majumdar, et al. [14] proposed an improved design of novel design of 2:4 decoders and has been used it to build a 3:8 decoder. The quantum cost of an n to 2^n decoder will be reduced by use of their 2:4 decoder blocks. As for n input signals, the number of output signal will be 2^n; still the increase in the number of gates will be linear in respect to the number of output signals. According to the author the proposed design uses Peres Gate, TR Gate and CNOT Gate A NOT gate is used to flip the output, which does not increase the quantum cost. The total quantum cost this design is 11.

In this paper 3:8 decoder is designed using 2:4 decoder block and Fredkin Gates with a quantum cost of 32 and 16 garbage outputs. And so to build 4:16 decoder, 8 extra Fredkin gates will be required so, the ultimate quantum cost of 4:16 decoder will be 71. Use of other gates such as TR gate, Peres, or Toffoli gate the number of gates will be twice as high also the quantum cost will be nearly doubled. In the same manner the number of garbage outputs for all these gates also increases. Since each Fredkin gate has one garbage output for this

architecture. Using the basic gates like Peres, TR or Toffoli cannot optimize the generalized design any further. Jugal Bhandari Geethanjali, Et al. in 2016 [15] investigated that new design approach consists of two Feynman gates, which has quantum cost of 1 each and four Toffoli gates, which are of 3x3 dimensions. This design has all parameters satisfied when compared to conventional designs with more constant inputs and less garbage outputs. This design requires a total of 6 gates, 6 constant inputs, 4 is garbage output. Design greatly improves over the conventional design of decoder using 3 Fredkin Gates in area power, delay. The improvements in these three metrics come at the cost of a slightly higher constant inputs and garbage outputs.

Nusrat Jahan Lisa, Et al. [3] designs a 2-4 decoder design generates all four necessary AND function using only one quantum Peres gate and three CNOT Gate so the number quantum gates circuit is seven. Then further designing a 3-to-8 decoder using only one the proposed 2-to-4 Quantum decoder circuit and four quantum Fredkin gates. A 4:16 decoder circuit consists of three 2-to-4 decoder circuits and eight quantum Fredkin gates, where the number of quantum gates of a quantum Fredkin gate is 5. So, the total number of quantum gates required constructing 4-to-16 decoder circuits. Also design has been constructed to show the power parameters and area constraints. Lafifa Jamal, Et al. in year 2015 [16] concluded 2:4 decoders using new reversible gate, namely HL gate. The proposed 2-to-4 decoder requires only one gate without any garbage output, which has 7 Quantum cost, the same gate count, garbage outputs and delay. But it has improved quantum cost while design is extended to reversible 3-to-8 decoder can be designed using one 2-to-4 reversible decoder and four Fredkin gates. The achievement of the design of 3-to-8 decoders is greater as the quantum cost 23, garbage output 1, constant input 6 in compare to previous design [11] in terms of garbage output, constant input and quantum cost. But 3:8 decoders are not much optimized in terms of other parameters.

V. ANALYSIS AND SCOPE OF WORK

The Proposed 2-to-4 and 3-to-8 reversible decoders are compared with their existing counterpart and are summarized in TABLE 2 and TABLE 3 units respectively. Comparision is done in terms of quantum cost, constant inputs, garbage outputs, number of gates, and reversible logic used for the implementation.

Researchers conclude that much work has not been done to reduce the quantum cost, delay, Area and power therefore further work can be done to reduce these parameters. The achievement of the design of 3-to-8 reversible decoder was greater with the existing one but design is not much optimized in terms of other performance parameters. We can use the energy recovery method, which uses reversible logic for power optimization. Also further work can be done by simulating the circuit on design architect to get more accurate result regarding power consumption. Exhaustive search method should be used to find the reversible gate with optimal solution, which produces the minimum quantum cost. Garbage outputs (outputs which are not used) should be kept as minimum as possible. Reducing the number of garbage outputs is one of the main task while using reversible logic.

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Table-2: Comparison of Various Parameters of 2-To-4 Decoders

2-to-4 Decoder Ref.	No. of Gates	Garbage Output	Quantum Cost	Contant Input	Reversible logic Gates
[15]	6	4	12	6	2 FG, 4 TG
[13]	4	1	12	2	2 FG, 2 FRG
[14]	5	1	11	3	1 PG, 1 TR, 3CNOT
[5,6]	3	2	12	4	1 F2G, 2 FRG
[12]	3	2	15	3	3 FRG
[11]	3	1	11	3	1 FG , 2 FRG
[3]	4	0	7	2	1 PG, 3 CNOT
[10]	1	0	8	2	1 FRG & Minimal reversible logic
[16]	1	0	7	2	HL Gate
Proposed	1	0	7	2	HL Gate

Table-3: Comparison of Various Parameters of 3-To-8 Decoders

3-to-8 Decoder Ref.	No.of Gates	Garbage Output	Quantum Cost	Constant Inputs
[15]	10	4	32	-
[13]	12	2	36	6
[14]	8	16	32	7
[5,6]	7	3	32	8
[12]	7	3	35	7
[11]	5	10	28	6
[3]	7	2	31	7
[10]	8	1	27	6
[16]	5	1	27	6
Proposed	5	1	23	6

VI. CONCLUSION

Decoder finds applications in low power digital designs, quantum computing, nanotechnology, DNA computing etc. The Main challenge of designing reversible circuits is to optimize the different parameters which result the design costly. In this paper we propose a novel design of a reversible 3-to-8 decoder that realizes appreciable improvement over existing ones in terms of quantum cost, garbage output, costant inputs, and number of gates. We found that the efficiency and Supermacy of the approach with several theoretical explanations it can be proved. However, further researcher interest may be to propose new gates that can be used to replace existing ones in higher dimensional decoders, resulting in decrease of quantum cost and other parameters.

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