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APPROACHES TO IMPROVE THE DYNAMIC CHARACTERISTICS OF CURRENT-STEERING DAC

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ABSTRACT

In this paper, explained the different types of DAC (Digital-to-Analog) architectures and their advantages and disadvantages. Mainly focused on current-steering digital-to-analog design for achieving high speed and high performance. The current-steering DAC is designed using binary weighted architecture. The benefits of this architecture is that it occupies less area, consumes less power and the number of control signals required are very less. The resolution of the DAC is 8-bits. The design of 8-bit current-steering DAC converts 8 most significant bits (MSBs) into their binary weighted equivalent, which controls 256 unit current sources. The performance of the DAC is measured using the static and dynamic parameters. In this paper mainly focussed on the dynamic performance characteristics like SNR (Signal to Noise Ratio) and SFDR (Spurious Free Dynamic Range. For measuring the dynamic parameters, frequency domain analysis is a better choice.

By implementing a technique in cadence, to increase the output impedance at higher frequencies. This technique is called as "complimentary current solution technique". This technique will improve the output impedance and SFDR compared to the normal unit element design. This technique contains mostly analog building blocks, like, current mirrors, biasing scheme and switching scheme and few digital blocks like D-ff (D-flip flop). The whole system is simulated and verified in MATLAB. Dynamic performances of the DAC such as SNR and SFDR are found with the help of MATLAB.

Keywords: DAC, D-FF, output impedance, SFDR, SNR, unit-element.

I. INTRODUCTION

Real-world analog signals such as temperature, pressure, sound, or images are routinely converted to a digital representation that can be easily processed in modern digital systems. In many systems, this digital information must be converted back to an analog form to perform some real-world function. The circuits that perform this step are digital-to-analog converters (DACs), and their outputs are used to drive a variety of devices. Loudspeakers, video displays, motors, mechanical servos, radio frequency (RF) transmitters, and temperature controls are just a few diverse examples. DACs are often incorporated into digital systems in which real-world signals are digitized by analog-to-digital converters (ADCs), processed, and then converted back to analog form by DACs. In these systems, the performance required of the DACs will be influenced by the capabilities and requirements of the other components in the system.

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A digital-to-analog converter (DAC) converts a digital signal to an analog, current or voltage, output. In today's telecommunication applications, for achieving good speed and performance at high frequencies, use of analog and mixed-signal circuits becomes very significant. In this report we have concentrated on the design of a current-steering DAC to meet the requirements [1].

In the telecommunication applications, high performance digital-to-analog converters (DACs) are used more, for e.g., the wireless local area networks (WLANs). In practice, for wireless communication, a current-steering DAC is suitable because of its high sample rate, efficiency of driving resistive loads and also due to low power consumption.

Now-a-days, for high speed and high performance, the usage of digital-to-analog converters (DACs) and analog-to-digital converters (ADCs) have extremely increased. In designing a DAC, two types of performance measures are important, namely, static and dynamic performance measures [2].

There are different kinds of architectures used to design the current-steering DACs. Mainly, there are three i.e., Segmented DAC, Thermometer coded DAC and Binary weighted DAC. Based on the requirements, binary weighted architecture is chosen for this design. This architecture is chosen for reducing the number of control signals and to reduce the power consumption [3].

The models are designed using MATLAB so that the simulation time is reduced for generating the input signal and for calculation of dynamic performances. The bandwidth used in this design is 500 MHz with a sampling frequency of 2 GHz and the required resolution is 8-bits.

In this thesis, we have discussed different approaches to reach a high output impedance at higher frequencies i.e., at gigahertz range and have also explained the importance of pole-zero analyses, in designing a higher output impedance at higher frequencies [3].

1.1 DYNAMIC PERFORMANCE ERRORS

These are more important for evaluating high speed DACs because they operate at increased frequency and sampling rate. The errors observed are settling time, glitches, and clock feed-through errors [4].

1.1.1 SETTLING TIME OF D/A CONVERSION:

Settling time is one of the important parameters for DACs. The time taken by DAC to reach 50% of lower significant bit of its new voltage or the final value based on the input code is called the settling time. It can be attributed to the slew time and delay time [5].

An example plot of settling time is shown in Fig. 1 [6].

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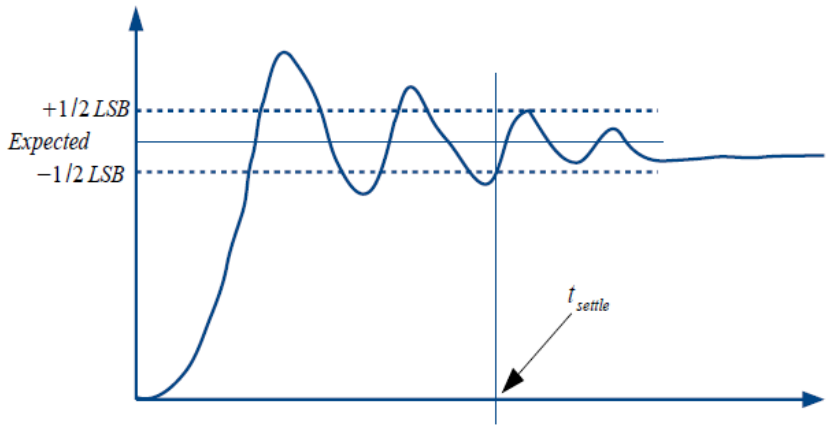

Figure 1: Settling time characteristic plot.

1.1.2 GLITCHES IN D/A CONVERSION:

Glitch energy is the time domain performance of DAC and it is one of the common specifications for high frequency DACs. The uncontrolled movement of DAC output from one value to a new value during the transition is called as glitch. Glitches occur due to the capacitive/inductive relation in the output of DAC [7]. During a short time period, false code will occur, for example if the code transition is 0111...1 then the output will be 1000...0. This is how glitches occur [2]. An example plot of DAC glitch energy with positive and negative glitches are shown in Fig. 2 [8]. The dots represent positive glitches and the dashes represent negative glitches. The Figure 2 shows glitches during the rising and falling edges of the signal.

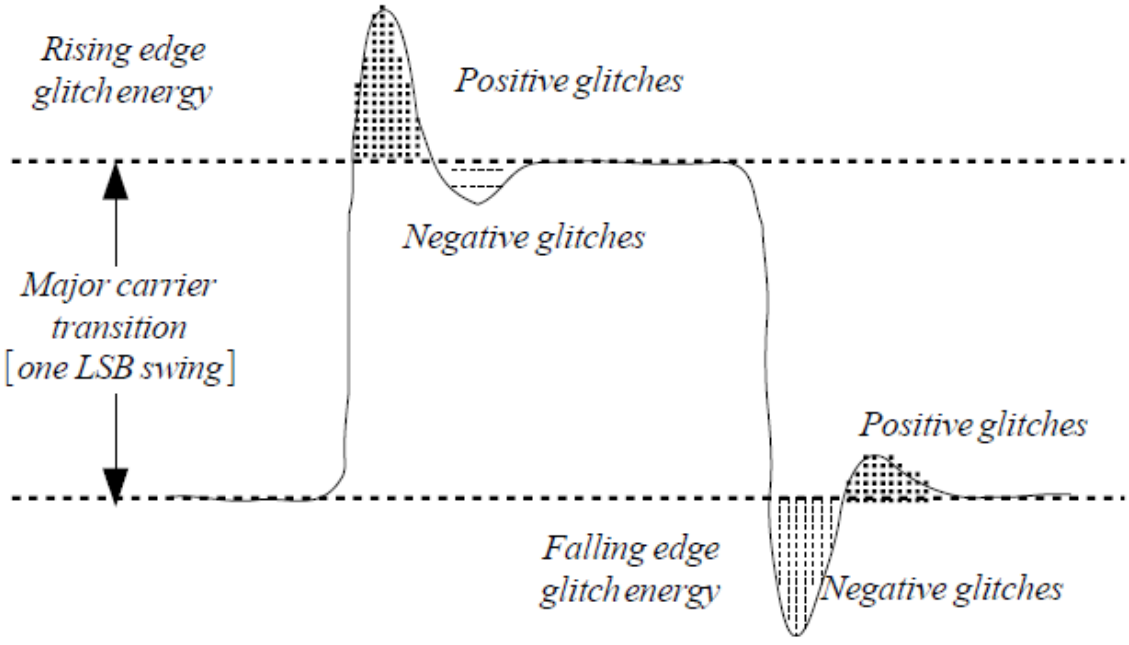

Figure 2: Glitch energy in DAC with positive and negative glitches.

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1.1.3 SIGNAL-TO-NOISE RATIO (SNR):

The signal-to-noise (SNR) is defined as the ratio of input signal power P_{signal} to the signal noise power P_{noise} within a particular band of frequency. Neglecting the harmonic components, the signal-to-noise formula is given by [3],

$$SNR = \frac{P_{signal}}{P_{noise}} \quad (1)$$

SNR is sometimes also expressed in dB scale i.e.

$$SNR = 10 \cdot \log_{10}\left(\frac{P_{signal}}{P_{noise}}\right) \quad (2)$$

This can also be written as,

$$SNR = P_{(signal,dB)} - P_{(noise,dB)} \quad (3)$$

1.1.4 SPURIOUS-FREE DYNAMIC RANGE (SFDR):

Spurious-free dynamic range ($SFDR$) is defined as the ratio of input signal power P_{signal} to that of the highest unwanted tone P_x in the frequency band and the formula is expressed in dB scale as,

$$SFDR = 10 \cdot \log_{10}\left(\frac{P_{signal}}{P_x}\right) \quad (4)$$

$$SFDR = P_{signal} - P_x \quad (5)$$

II. BINARY-WEIGHTED DAC ARCHITECTURE:

This type of DAC architecture utilizes a number of current sources, resistors or capacitors. These elements are always binary weighted. The DAC output in static case can be written at the time instant *nT* is

$$A(nT) = A_{os} + A_0 \cdot \sum_{m=1}^{N} 2^{(m-1)} \cdot b_m(nT) \quad (6)$$

From the equation (6) *A*0 is gain reference, *AOS* is an offset reference, *bm*信*nT* 商∈ 0,1 ,1≤*m*≤*N* are the input bits, update period is denoted as *T* . The architecture of binary weighted DAC as shown in Fig. 3 [9].

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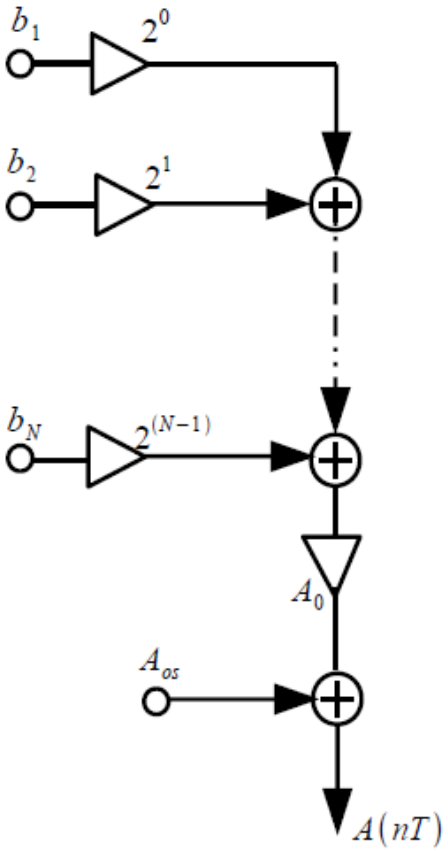

Figure 3: Binary weighted DAC architecture

This architecture consists of lot of advantages like, number of switches are less and digital decoding circuits are always kept at minimum. But it has some disadvantages, like ff the number of bits increases then the weights of MSB and LSB difference is large, so the DAC becomes sensitive to glitches and mismatch errors and monotonicity is not guaranteed [9].

Binary weighted DAC is one of the architecture using now-a-days for high speed and high performance DACs.

III. CURRENT-STEERING DAC:

In CMOS technology, this current switching technique is the natural choice, because the elements present in this DAC are easy to implement. The elements are only wire connections for summing elements. A binary weighted current-steering DAC is shown in Fig. 4 [9].

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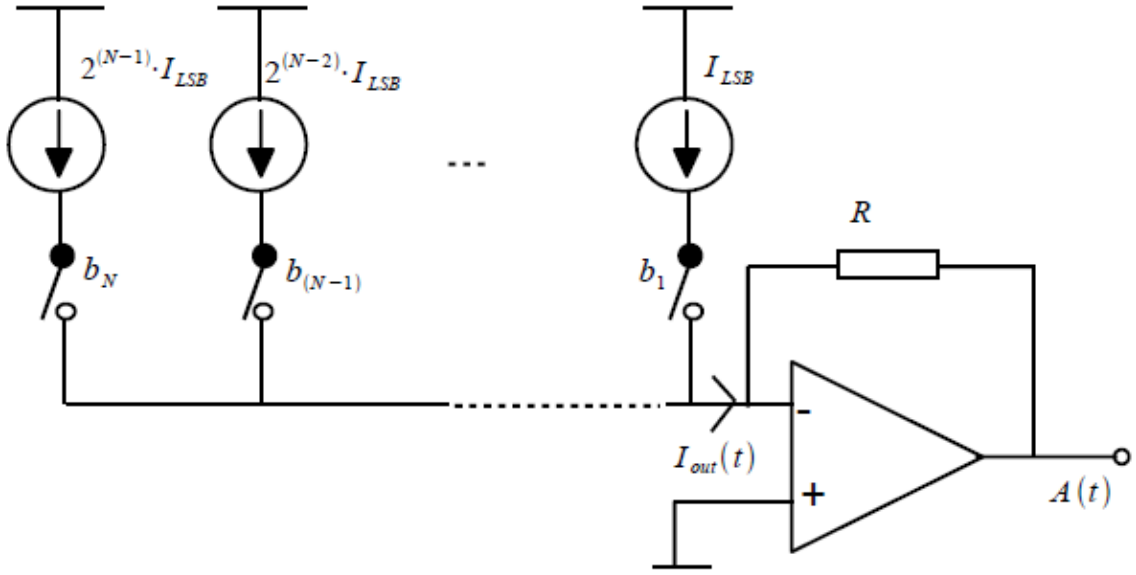

Figure 4: N-bit current-steering DAC.

The $b_1, b_2 \ldots b_N$ are the input bits, those bits will control the switches. The output current is given by

$$I_{out}(X) = 2^{(N-1)} I_{LSB} \cdot b_N + \cdots + 2I_{LSB} \cdot b_2 + I_{LSB} \cdot b_1$$

The third harmonic distortion due to SFDR is

$$SFDR = \frac{20 \cdot \log \cdot (64 \cdot B^6 + 48 \cdot B^4 + 40 \cdot B^2 + 35)}{(16 \cdot B^4 + 20 \cdot B^2 + 21)}$$

If the output impedance increases, then the SFDR also increases simultaneously, because SFDR is directly proportional to output impedance .

ADVANTAGES:

➢ SFDR increases compared to other techniques.

➢ Matching between main and complimentary current branches.

Based on the all techniques, the complimentary current solution is the best solution to improve the output impedance and SFDR at higher frequencies.

IV TEST-BENCH AND SCHEMATIC OF COMPLEMENTARY CURRENT SOLUTION TECHNIQUE

The schematic and test-bench for complementary current solution technique is shown in Fig. 5 and Fig. 6.

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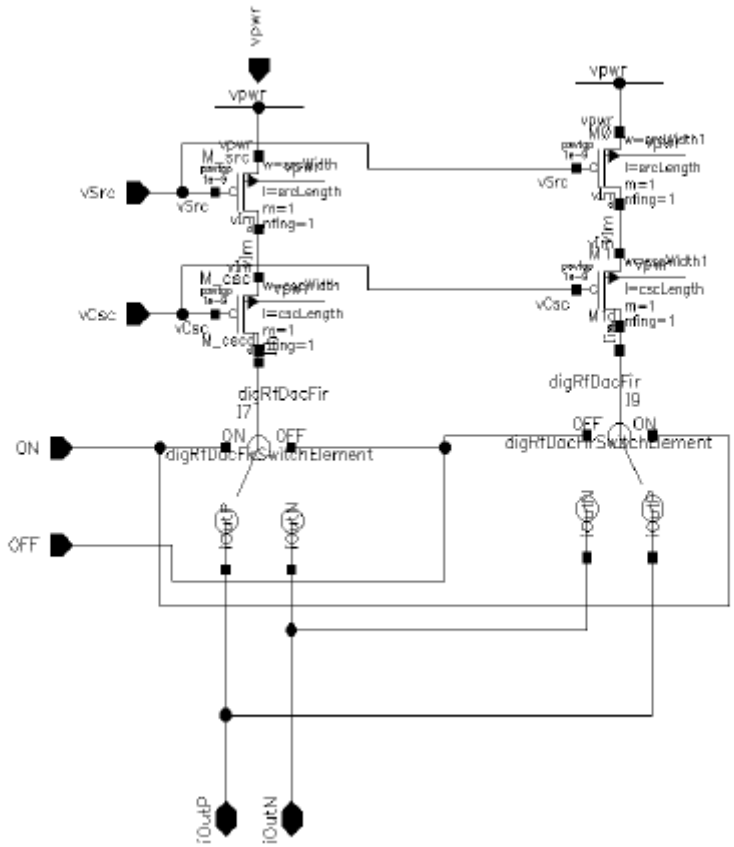

Figure 5: Schematic view of complementary current solution

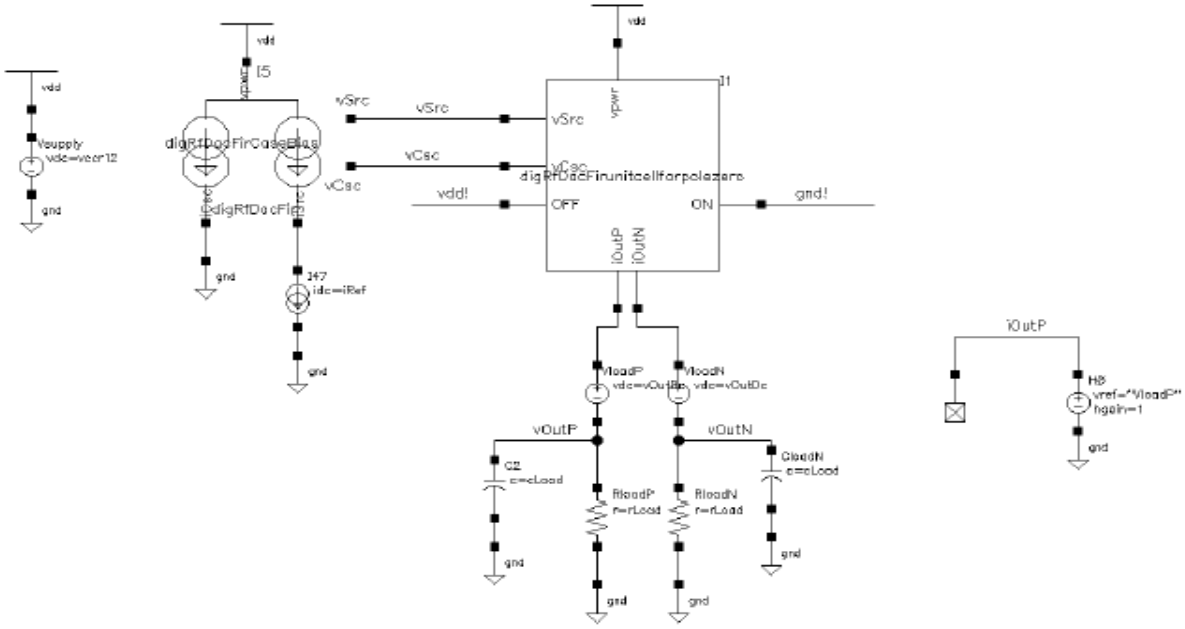

Figure 6: Test-bench of complementary current solution technique

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V SIMULATION RESULTS

The complementary current solution technique is simulated and tested in cadence 6.15 version by variation of transistor sizes for obtaining the high output impedance at higher frequencies. The result wave forms are shown in Fig.7. In Fig. 7 red colour implies SFDR and blue one shows output impedance.

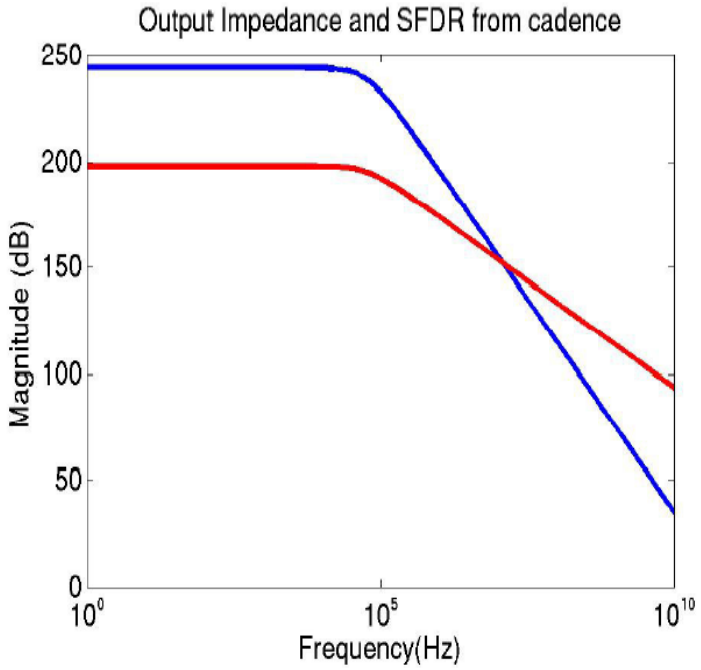

Figure 7: SFDR and Z out plot for complementary current solution technique.

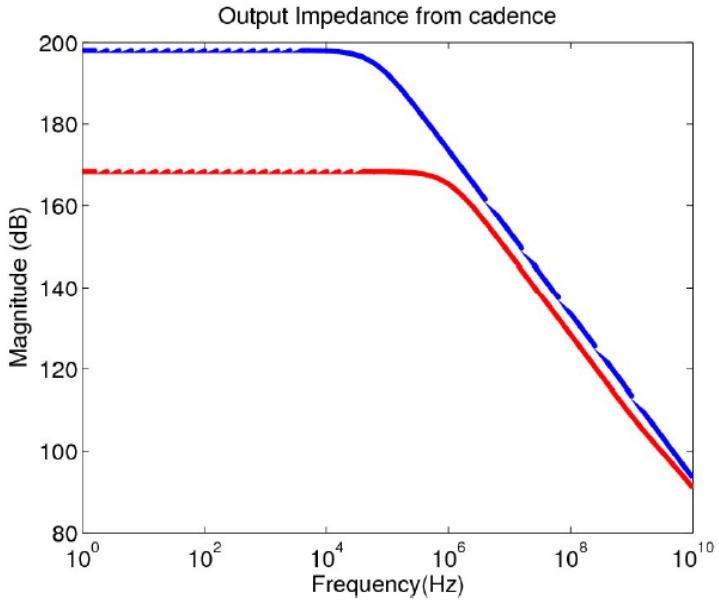

Figure 8: Z_out for cascode and complementary current sources.

Output impedance variation between the normal cascode transistors and complimentary current solution circuit is shown in Fig. 8. In the plot, blue colour implies *Zout* of complementary current solution and red colour implies *Zout* of cascode current source technique. This plot shows that the output impedance is increased by 5

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dB at 1 GHz frequency in complimentary current solution technique as compared to normal cascode current source.

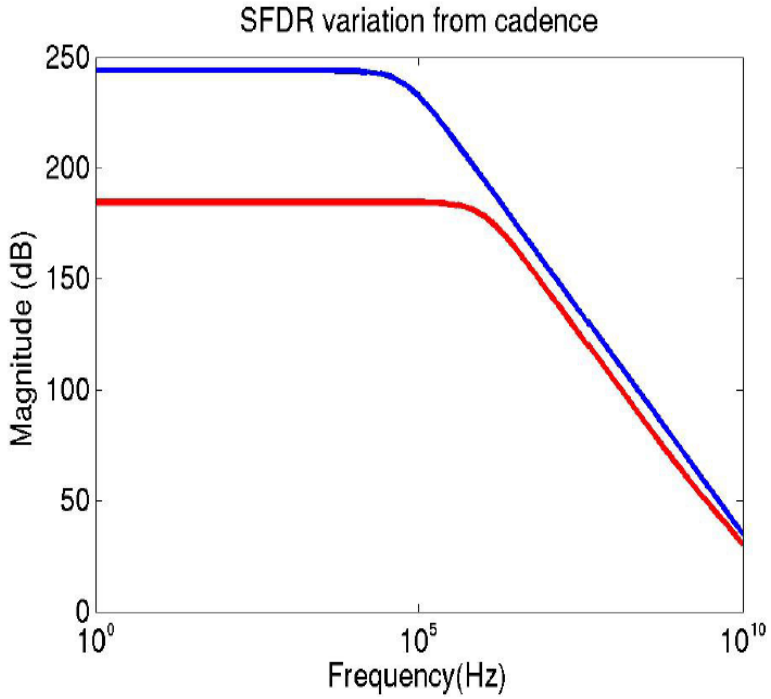

Figure 9: SFDR variation for normal cascode and complementary current circuits.

SFDR variation between the normal cascode transistors and complimentary current circuit is shown Fig. 9. In Fig. 9 blue colour implies complementary current solution SFDR and red colour implies to cascode current source circuit. From Fig 9, the SFDR is increased by 10 dB in the complimentary current solution technique compared to normal cascode transistor technique.

VI. CONCLUSION

This paper explains the design of current-steering DAC using binary weighted architecture for achieving high speed and high performance at higher frequencies. This architecture has a lot of advantages over other techniques such as low cost, because there are no op-amps in this design and power efficiency is high since all the power is directed to the output.

The proposed architecture contains several sub blocks such as unit-element, D flip-flop, switching scheme, biasing scheme and all these blocks are designed in cadence version 6.1.5 environment. The cascoded current source is implemented for achieving the high-output impedance. Wide swing current mirror is chosen for biasing purpose because, it is good in low voltage applications and also for high-output impedance applications.

This design (current-steering DAC) is useful in many applications, such as high speed, high performance and most of the telecommunication and mixed signal applications. This paper mainly focuses on a unit-element, for achieving the high-output impedance. Output impedance was improved at higher frequencies. Based on this, the parameters that affect the output impedance and the dominant pole were found. Complimentary current solution

technique was implemented in cadence for improving the output impedance. The objective of this architecture is to increase the output impedance at higher frequencies. This architecture has given best results at higher frequencies in the giga-hertz range.

VII FUTURE WORK

The work done in this paper can be taken forward using some of the ideas mentioned below. Advanced current mirroring techniques can be used to implement the bias circuitry, since wide swing current mirror used in this work will not accurately copy the current due to drain- source voltage variations.

Other techniques like, charge removal replacement technique, current switch driver and current source design technique, output impedance linearization technique, etc., can also be tried and analysed to improve the output impedance at higher frequencies, with the help of pole and zero modification/manipulation, since the complimentary current solution technique improves SFDR only 10dB at higher frequencies.

To improve the dynamic performances of the DAC, a filter can introduced after the DAC. It will help to reduce noise. To improve output impedance, we used a simple differential switch in our case. Better switching techniques like dummy transistors, bootstrapping technique, etc., can be tried. The next level is to do the layout. Layout simulations can be performed and those layout results can be compared with transistor level results and see the difference between transistor level result and layout level result.

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M.Niraja was born at Chittoor, AP, and India. She completed her B.Tech degree from Sri Venkateswara College of Engineering & Technology, Chittoor, Ap, India in 2009, and MS in 2013 from Linkoping University, Linkoping, Sweden in Communication Electronics as specialization She is currently working as a Assistant Professor in Department of ECE in Siddharth Institute of Engineering & Technology, Puttur, AP, India. Her research interest includes RF Design, Wireless communication, and embedded design.

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