



SIMULATION AND EXPERIMENTAL EVALUATION OF VARIABLE SPEED INDUCTION MOTOR DRIVE FED BY VSI AND STUDY OF CURRENT HARMONICS UNDER STEADY STATE CONDITIONS

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ABSTRACT

In earlier days the Induction Motor (IM) is considered to be constant speed motor. In almost all the industries the work horse power is the IM. But due to the advances in computer technology the speed of the IM can be varied within certain constraints. The 2-level inverter is used and is controlled by the Arduino microcontroller board using the space vector modulation (SVM) technique. It is fact that in this method the output of the inverter will not be sinusoidal and hence at the star point of the load there exists a Common Mode Voltage (CMV), it produces Electromagnetic interference (EMI) and causes the disturbance to the nearby communication and measuring devices. In this paper the authors have discussed the harmonics of the line current under steady state conditions. Simulation has been carried out using MATLAB/Simulink and validated using the experimental work. The voltages and currents are recorded using Agilent make mixed signal oscilloscope (MSO). Fast Fourier transform (FFT) has been done using the signal Analysis software and results are plotted with frequency versus voltage and current so that the same results can be compared with Federal communication committee (FCC) and special committee on radio interference (CISPR) standards.

Keywords: Common Drive Mode Voltage, Space Vector Modulation, Voltage Source Inverter, Variable Speed Induction Motor.

I. INTRODUCTION

The phenomena of current harmonics in adjustable speed drive systems using converter-inverter is due to the existence of CMV and also by fast switching ON and OFF of power electronic devices used in inverters. The existence of CMV has been reported by B.Muralidhara etal [1]. It produces EMI and causes the disturbance to the nearby communication & measuring devices [2]. The current harmonic analysis of inverter fed IM drive system [3]. Shaft voltages and their resulting currents were recognized by Alger in the 1924's [5]. The asymmetrical flux, through the arbour line loop (the shaft loop), induces CMV. In 1996, Chen [6] identified the capacitive CMV between stator and rotor due to a switch-mode variable speed motor drive. Annette Muetze etal [7] reports that, the

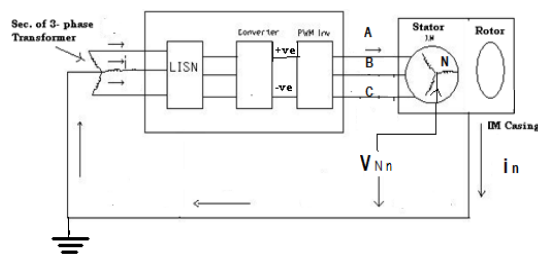
high-frequency (HF) component exists at the common mode voltage. Hence it is necessary to reduce the CMV within limits [4] so that there will be reduced heating and less insulation problem of the winding.

The three phase inverter is widely used in variable speed AC 3phase IM drive System, produces three phase AC output voltage of desired amplitude and frequency from a fixed DC voltage source. In two level inverter, it has levels of voltages $[\pm 2/3V_{dc}, \pm 1/3V_{dc}]$, hence the output waveform of two level inverter is stepped square wave. For efficient operation, the output waveform of an inverter should be sinusoidal. The square wave output contains harmonics to reduce the harmonics in the output of the inverter the multilevel inverter concept is widely used.

T A. Nabae et al [8] has discussed about Multi level inverter (MLI) concept in 1981. There are advantageous in terms of power quality, EMI, with low switching losses used in medium and high voltage applications using MLI. The disadvantages are the number of power semiconductor devices, complexity in circuits and different DC voltage levels. The Arduino [9] board is used to generate the switching pulses as per the Hexagon of the SVM.

II. COMMON MODE VOLTAGE IN INVERTER DRIVEN AC INDUCTION MOTOR

In a three –phase AC system, the CMV can be defined as the voltage between the common ground and the star point of the load. It is important to define the CMV in mathematical terms in order to compare its characteristics among different types of source and load combinations. In three-phase AC loads, the phase to ground voltages can be written as the sum of the phase voltages and the voltage across the star point of the load to the star point of the source power supply. Since in a balanced system, the sum of all three phase-to-neutral voltages is zero, the voltage from the neutral to ground (CMV) can be defined in terms of phase to ground voltage as shown in Fig.(1).



$$: V_{A-n} = V_{AN} + V_{N-n} \quad (1)$$

$$: V_{B-n} = V_{BN} + V_{N-n} \quad (2)$$

$$: V_{C-n} = V_{CN} + V_{N-n} \quad (3)$$

For balanced three phase load $\sum V = 0$

$$: V_{AN} + V_{BN} + V_{CN} = 0 \quad (4)$$

$$: V_{N-n} = [(V_{A-n} + V_{B-n} + V_{C-n}) / 3] \quad (5)$$

Fig.1: Schematic diagram of Inverter fed IM with Common Mode Voltage as EMI source.

III. THE PROPOSED WORK

Simulation, experiment of two level inverter using SVM for the speed control of induction motor has been done, with measurement of CMV, Phase voltage, line current, sum of phase currents using MSO associated with isolation module, high frequency current probe and Hall effect sensor. The inverter is built using the IGBT/MOSFET devices, DC link capacitors and other electronics components.

SVM methodologies have the advantages of more output voltage when compared to sine triangle pulse width modulation (SPWM) method [10]. The advantage of using the SVM is that the gating signal of the power devices can be easily programmed using μ -controller/digital signal processor (DSP) and offers improved dc bus utilization [11], reduced switching losses and lower total harmonic distortion.

IV. EXPERIMENTAL SETUP

In the inverter, the IGBT/ MOSFET are used as devices with necessary snubber circuit. The μ -controller output after isolation is given to the gate of the devices ([12], [13] and [14]). The μ -controller is programmed for different frequencies and the typical output of the μ -controller is given in the Fig. (4b). In addition, necessary isolation module, high frequency current probes and Line Impedance Stabilization Network (LISN) are used for sensing and measuring the parameters in the experimental work. While running the IM the phase voltage, line voltage, line current, sum of phase current and the CMV are recorded using Agilent MSO/DSO for further analysis. The necessary FFT has been done in simulation using MATLAB/Simulink and also for the experimental results using Origin signal Analysis software. At the end the results are discussed showing the steady state current harmonics content in different frequencies viz. 30Hz, 40Hz and 50Hz. The Fig.1 shows the schematic diagram, the simulation and the experimental circuits shown in Fig. (2, 3).

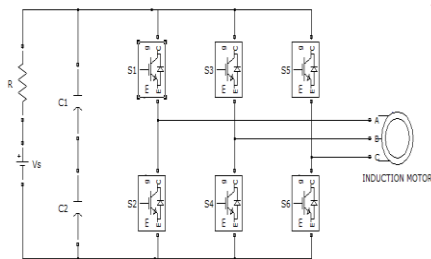


Fig.2 Simulation Circuit diagram

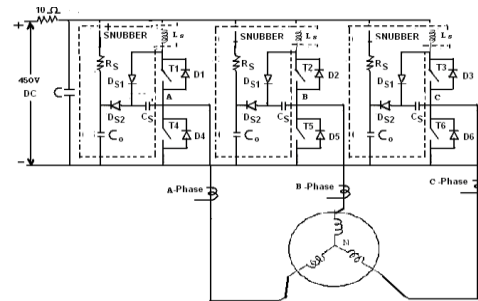


Fig. 3 Experimental set up Circuit diagram

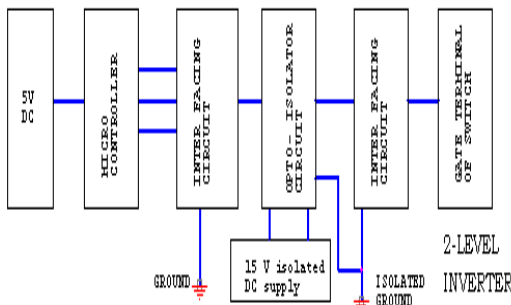


Fig. (4a).Block diagram of gate drive circuit micro controller

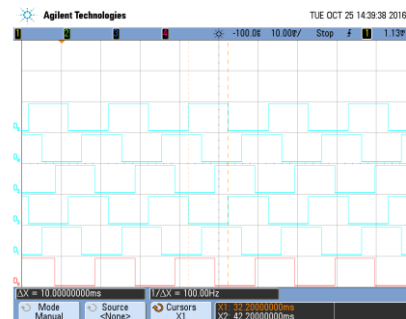


Fig. (4b).Gate pulses generated for Inverter using micro controller

4.1 Simulation: The MATLAB is used to simulate the circuit shown in the Fig.2. The results are given in the Fig. (5a, 5b).

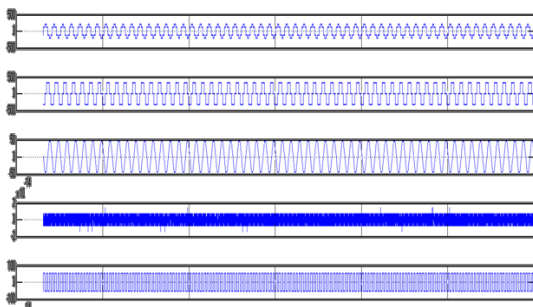


Fig. (5a): Simulation (Inverter output 50Hz. 2Sec.)

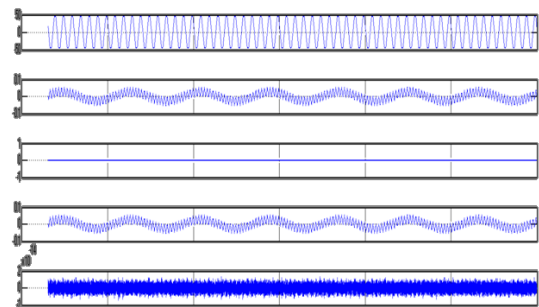


Fig. (5b): Simulation (Inverter output 50Hz. 2Sec.)

[Top to Bottom]

CH-1: Phase Voltage, CH-2: Line Voltage,
CH-3: Line Current, CH-4: Common Mode Voltage,
CH-5: Sum of Phase Currents.

[Top to Bottom]

CH-1: Line Current, CH-2: Sum of Phase Currents,
CH-3: Common Mode Voltage, CH-4: C.M. Current,
CH-5: Sum of ([CH-2] - [CH-4])



Fig. (5c). Experimental Setup

V. EXPERIMENTAL RESULTS

The experimental circuit is shown in Fig.3, the block diagram of the gate drive circuit and the gating pulses generated by the microcontroller shown in Fig. (4a, 4b). The photograph of the experimental setup is shown in Fig. (5c). The phase voltage, line current, line voltage, common mode voltage, the sum of phase currents and common mode current are recorded and is shown in Fig. (6a, 6b).

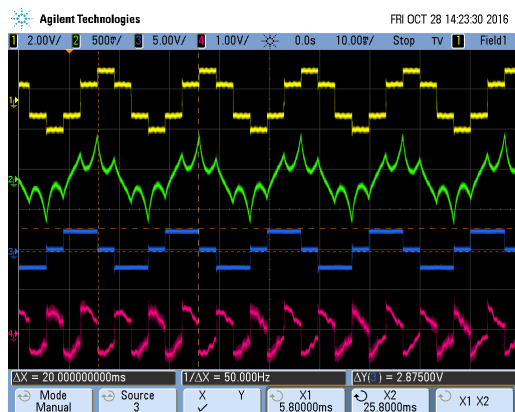


Fig. (6a). Inverter output waveforms
CH 1: Phase Voltage [200:1], CH 2: Line Current [1:1]
CH 3: Line Voltage [200:1], CH 4: C.M. Voltage [200:1]



Fig. (6b). Inverter output waveforms
CH 1: Sum of Phase Current [1:1]
CH 4: Common Mode Current [1:1]

5.1 Results and discussion

The even harmonics and its multiples will be zero since there is symmetry of waveform. The odd triplen harmonics (i.e., 3rd, 6th, 9th harmonic order, etc.) are cancel out each other since it circulates in the transformer windings and will not appear in the load. The only harmonics present are 5th, 7th, 11th, 13th and 17th etc. The harmonic magnitude of voltage will not produce useable torque in drive system and at the same time it produces heat which is harmful to the winding insulation. Fig. (7a-7d) shows the simulated FFT of phase voltage using the MATLAB and in the Fig. (8a-8d) shows the FFT from experiment using Origin software. Fig. (9a-9f) shows the simulated FFT of Line current

using the MATLAB and Fig. (10a-10f) shows the FFT Line current from experiment using Origin software. Fig. (11a-11d) shows the simulated FFT of CMV using the MATLAB and Fig. (12a-12d) shows the FFT CMV from experiment using Origin software. Fig. (13a, 13b) shows the simulated FFT of sum of phase current using the MATLAB and Fig. (13c, 13d) shows the FFT sum of phase current from experiment using Origin software.

5.2 Figures & Graphs

Fig. (1, 2, 3 & 4) shows the block diagram, Fig. (5c) shows the experimental setup and Fig. (6a, 6b) shows the CRO recordings. Fig. (5a, 5b), (7a-7d), (9a-9f), (11a-11d) and (13a, 13b) are shows the MATLAB simulated results. Fig. (8a-8d), (10a-10f), (12a-12d) & (13c, 13d) shows the experimental FFT results using Origin signal Analysis software.

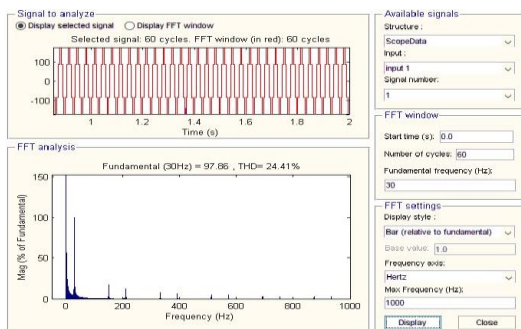


Fig.7a: (30Hz) FFT of Phase Voltage scale

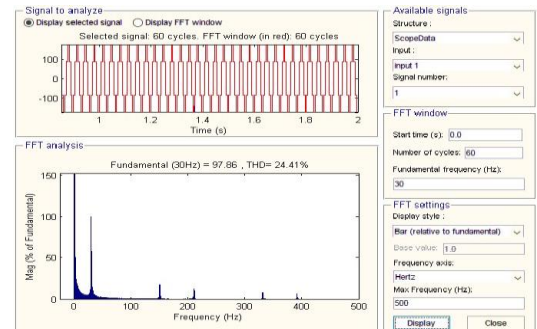


Fig.7b: (30Hz) FFT of Phase Voltage with reduced scale

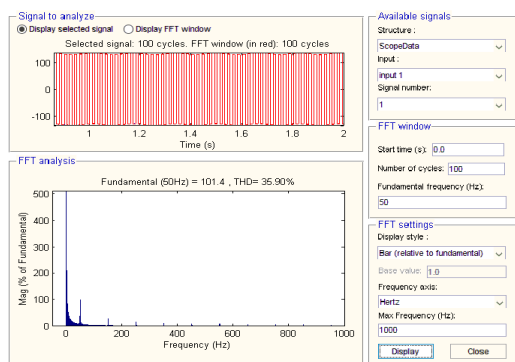


Fig.7c: (50Hz) FFT of Phase Voltage

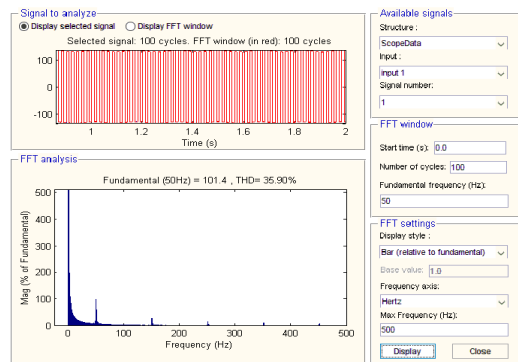


Fig.7d: (50Hz) FFT of Phase Voltage with reduced scale

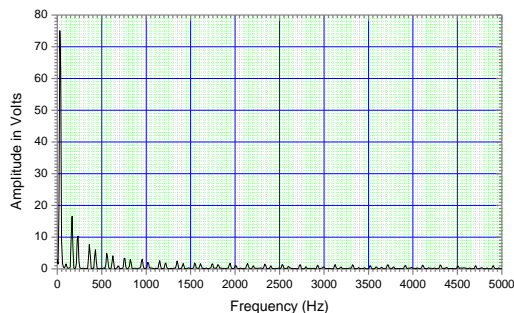


Fig.8a: (30Hz) FFT of Phase Voltage

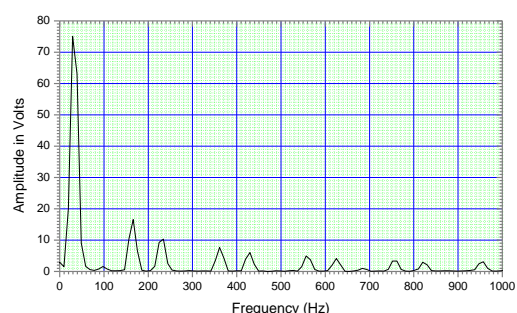


Fig.8b: (30Hz) FFT of Phase Voltage with reduced scale

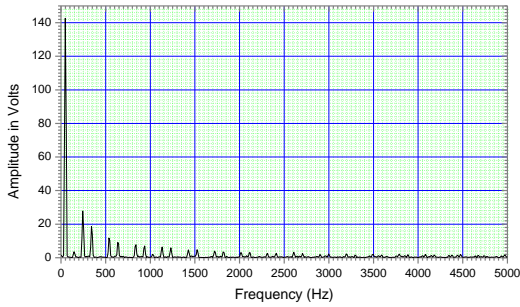


Fig.8c: (50Hz) FFT of Phase Voltage

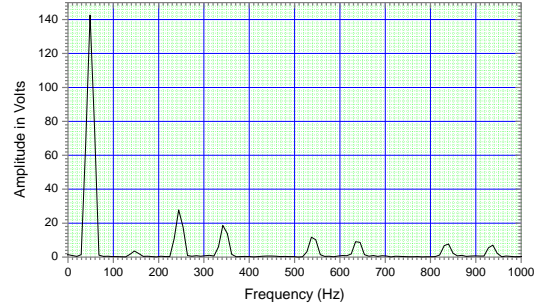


Fig.8d: (50Hz) FFT of Phase Voltage with reduced scale

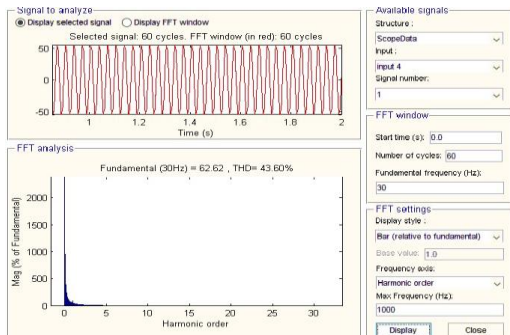


Fig. 9a: (30Hz) FFT of Line Current

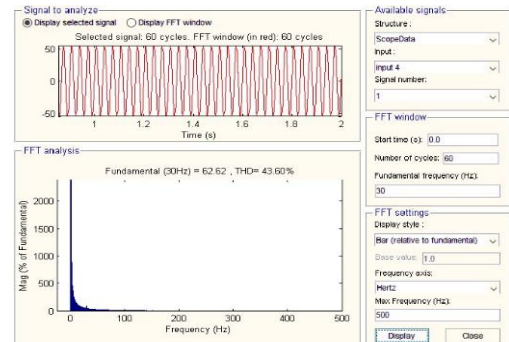


Fig. 9b: (30Hz) FFT of Line Current with reduced scale

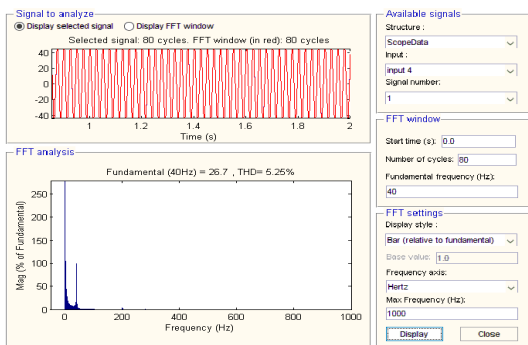


Fig. 9c: (40Hz) FFT of Line Current

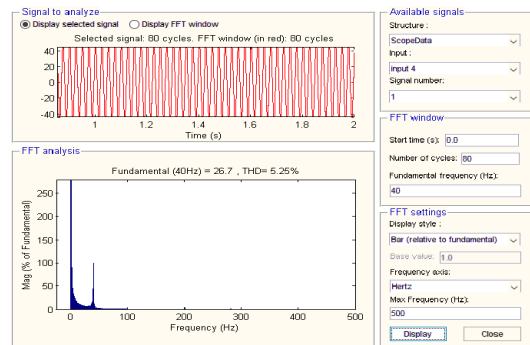


Fig. 9d: (40Hz) FFT of Line Current with reduced scale

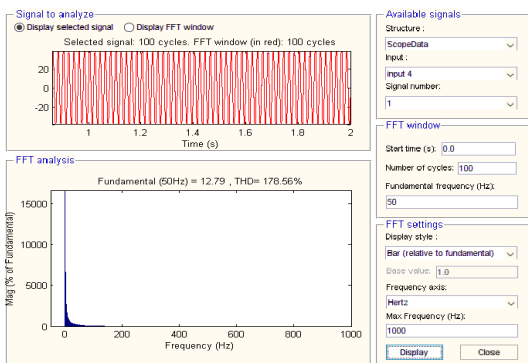


Fig. 9e: (50Hz) FFT of Line Current

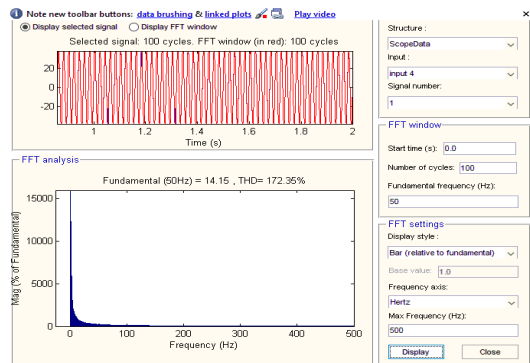


Fig. 9f: (50Hz) FFT of Line Current with reduced scale

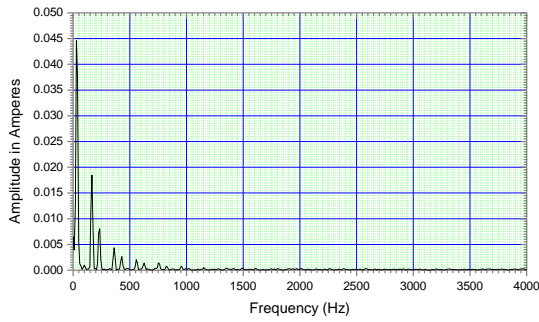


Fig. 10a: (30Hz) FFT of Line Current

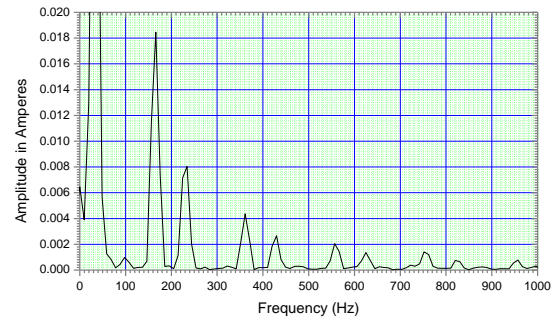


Fig. 10b: (30Hz) FFT of Line Current with reduced scale

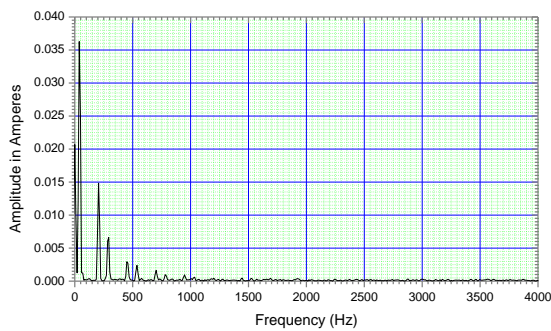


Fig. 10c: (40Hz) FFT of Line Current

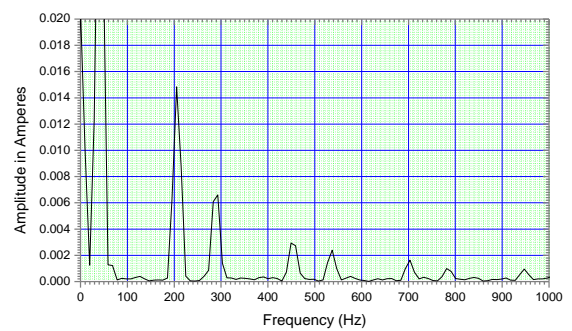


Fig. 10d: (40Hz) FFT of Line Current with reduced scale

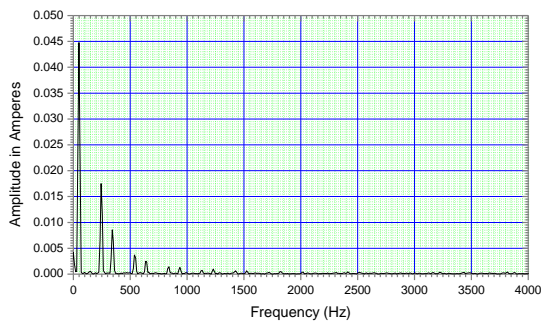


Fig. 10e: (50Hz) FFT of Line Current

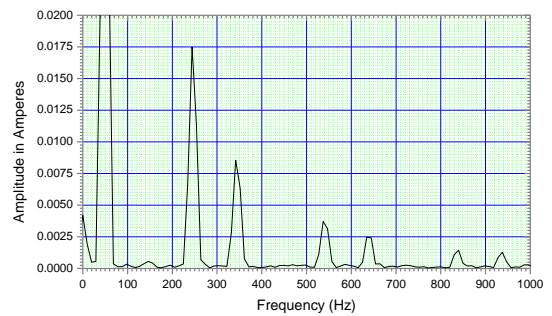


Fig. 10f: (50Hz) FFT of Line Current with reduced scale

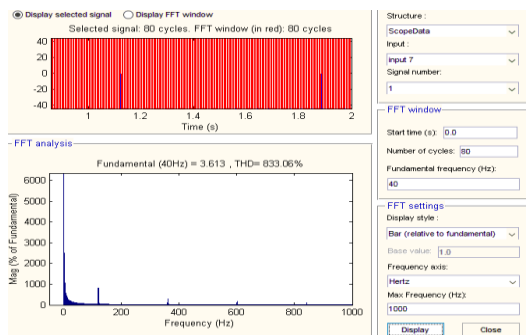


Fig. 11a: (40Hz) FFT of C.M. Voltage

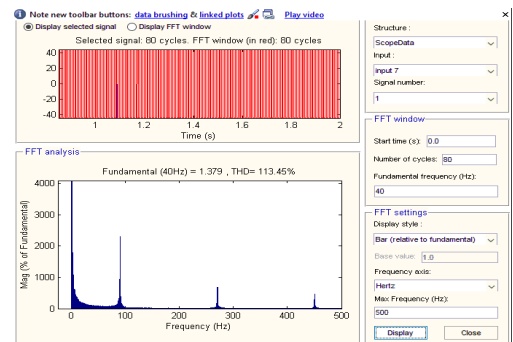


Fig. 11b: (40Hz) FFT of C.M. Voltage with reduced scale

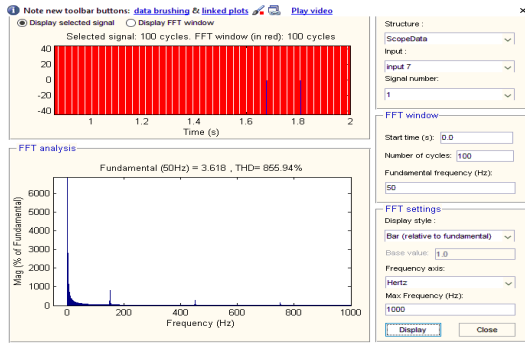


Fig.11c: (50Hz) FFT of C. M. Voltage

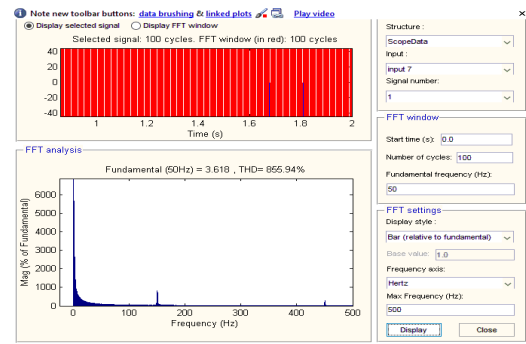


Fig.11d: (50Hz) FFT of C.M. Voltage with reduced scale

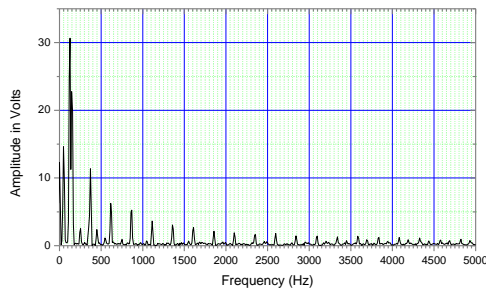


Fig.12a: (40Hz) FFT of C. M. Voltage

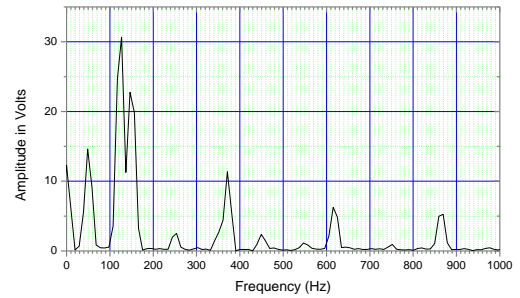


Fig.12b: (40Hz) FFT of C.M. Voltage with reduced scale

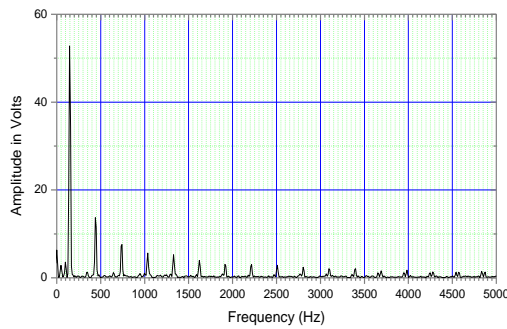


Fig.12c: (50Hz) FFT of C. M. Voltage

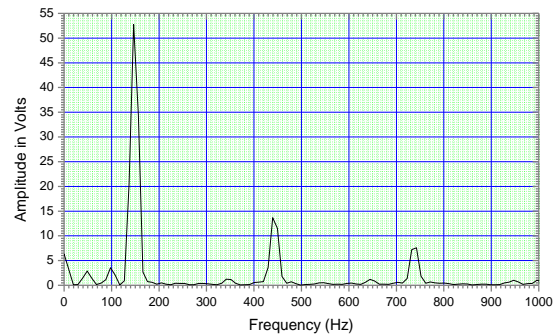


Fig.12d: (50Hz) FFT of C.M. Voltage with reduced scale

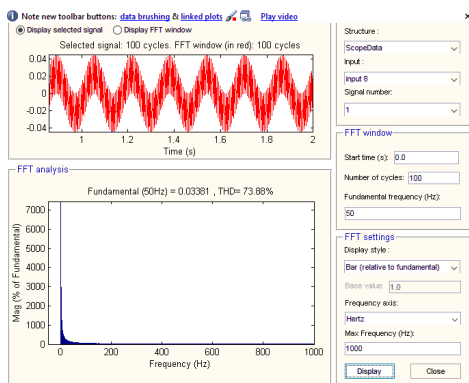


Fig.13a: (50Hz) FFT of Sum of Phase Current scale

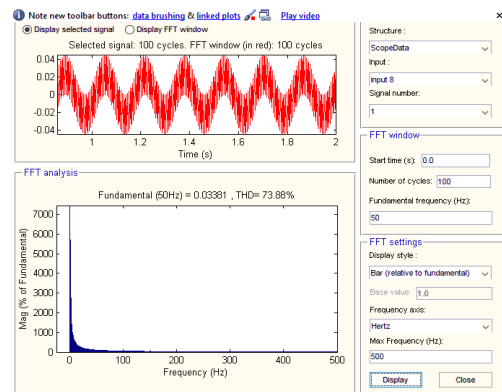


Fig.13b: (50Hz) FFT of Sum of Phase Current with reduced scale

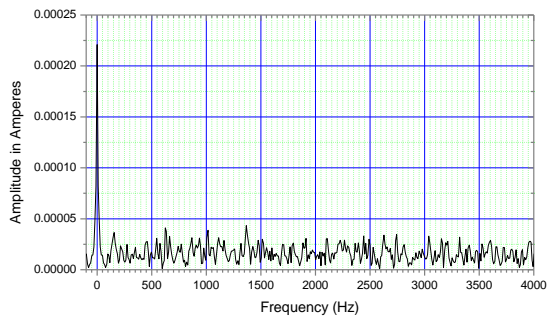


Fig.13c: (50Hz) FFT of Sum of Phase current

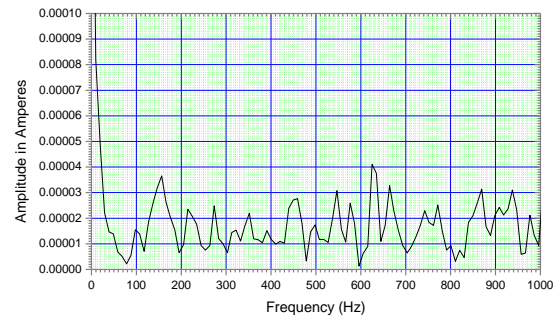


Fig.13d: (50Hz) FFT of Sum of Phase current with reduced scale

VI. CONCLUSION

This paper presents a 3phase two level VSI fed IM drive system to analyze the harmonic components of the output voltage and current. It is to be noted that the phase voltage harmonics and the line current harmonics under steady state conditions in simulation and the experimental are the same as (5th, 7th, 11th 13th etc),. The amplitudes are diminished when the harmonics frequency increases. It is observed that in the CMV the harmonic frequencies are 3times the fundamental frequency of 50Hz (150, 450, 750Hz etc) shown in simulation in Fig. (11d) and experiment result shown in Fig. (12d). Fig. (6b) shows the sum of phase current (CH 1) and the common mode current (CH 4) are in phase and in magnitude. Also in the simulation and experimentation, in the FFT analysis, the sum of phase current shows the same values. Hence it is concluded that the simulation is validated with the experimental work.

VII. ACKNOWLEDGEMENT

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Dr.V.Muralidhara obtained his B.E, and M.E degrees from University of Mysore and earned Ph.D. from Kuvempu University. He has a teaching experience of over 40 years inclusive of research as a par at of his Ph.D. Started his teaching career at PES College of Engineering Mandya, served there for 6 years and served for 31 years at Bangalore Institute of Technology [BIT], Bangalore and retired from there as Prof. & Head of EEE. Presently working as an Associate Director at Jain University. His area of interest is Power Systems and HV Engineering. In his credit he has 10 papers published in reputed International conferences and one paper in a Journal. At Present he is guiding five doctorate scholar.