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A NOVEL DESIGN OF 6-BIT FLASH ADC DESIGN WITH OPTIMIZED POWER CONSUMPTION

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ABSTRACT

Analog-to-Digital converters are essential building blocks in modern electronic systems. Most of the mixed signal systems today require analog to digital converters and they are being used at the front-end along with DSP applications integrated into one single chip using CMOS technology. Latest VLSI design trend for signal processing system demands high speed operation and less power consumption. A flash ADC architecture is the faster among known ADC architectures, but limited to lower resolution due to large number of components and high power dissipation. So the flash ADC using NMOS Resistor ladder, latched-based comparators, buffer and encoder technique requires. In the digital domain, low power consumption, high speed and low voltage requirements are becoming more important issues these issue solved by use in CMOS technology. The NMOS Resistor ladder, latched-based comparators, buffer and encode technique allows faster ADC. Latched based comparators have been used to provide 6 bits output flash ADC code with low resolution, high speed & low power consumption. The cascode is a two-stage amplifier composed of a transconductance amplifier followed by a current buffer with weighted currents have been used to enhance sampling rate. In this paper, the proposed circuit is designed NMOS Resistor ladder, latched-based comparators, buffer and encoder technique and simulated with the help of TANNER-EDA tool in 45nm CMOS technology.

Keywords: NMOS Resistor Ladder, Latched Comparators, Buffer And Encoder.

I. INTRODUCTION

Analog-to-Digital converters are essential building blocks in modern electronic systems. Most of the mixed signal systems today require analog to digital converters and they are being used at the front-end along with DSP applications integrated into one single chip using CMOS technology. Latest VLSI design trend for signal processing system demands high speed operation and less power consumption. A flash ADC architecture is the faster among known ADC architectures, but limited to lower resolution due to large number of components and high power dissipation. So the flash ADC using NMOS Resistor ladder, inverter-based comparators, buffer and encoder technique requires 2n-1 comparators for an n-bit A/D converter. The NMOS Resistor ladder, latched -based comparators, buffer and encode technique allows faster A/D conversion speed using the standard CMOS logic circuitry preferred for SOC implementation.

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ADCs should be integrated with digital circuits on a single chip for the portable devices. All battery powered devices are now being designed to include low power techniques to long the battery life. ADCs need low power architecture or a low power technique. Low voltage operation is one of the difficult challenges in the mixed-signal ICs. This paper describes NMOS Resistor ladder, latched-based comparators, buffer and encoder using CMOS technology for generating threshold voltage levels for 6-bit CMOS flash ADC with an alternative technique for high speed and for variable resolution, low power consumption.

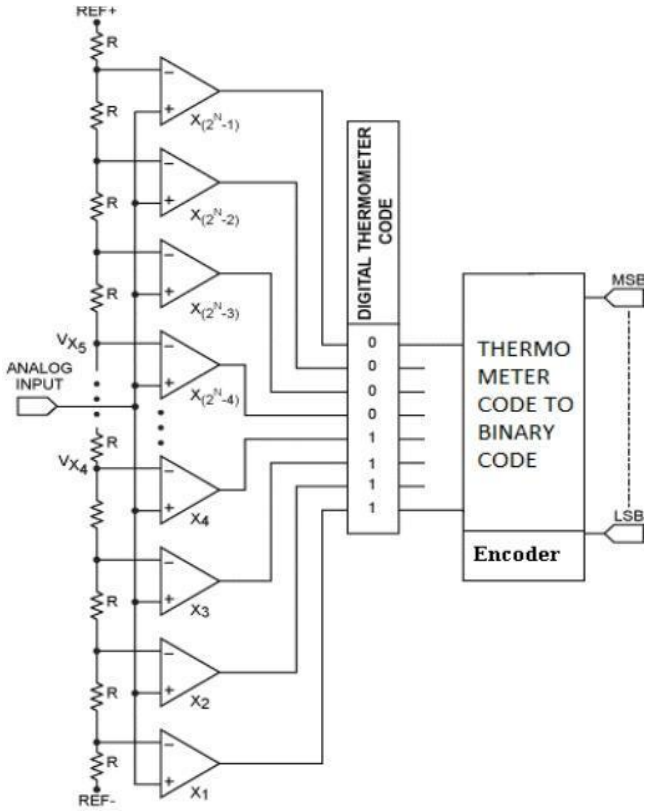

Fig.1 Generic block diagram of Flash ADC

II. NMOS RESISTOR LADDER

In a flash Analog-to-Digital Converter, resistor ladder block is used to generate the reference voltages for the comparators. In this we use NMOS as a resistor. It is the good choice for resistor ladder because the NMOS resistor requires less area as compared to any type of resistor but NMOS resistors behave as a non-linear resistor. So the design challenge of NMOS resistor, NMOS is work in the linear region.

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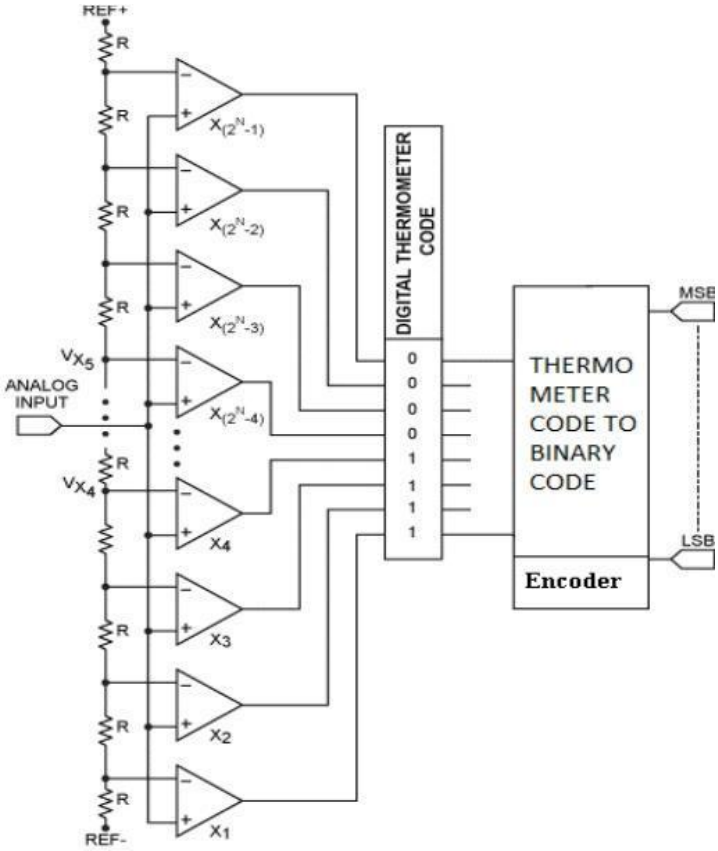

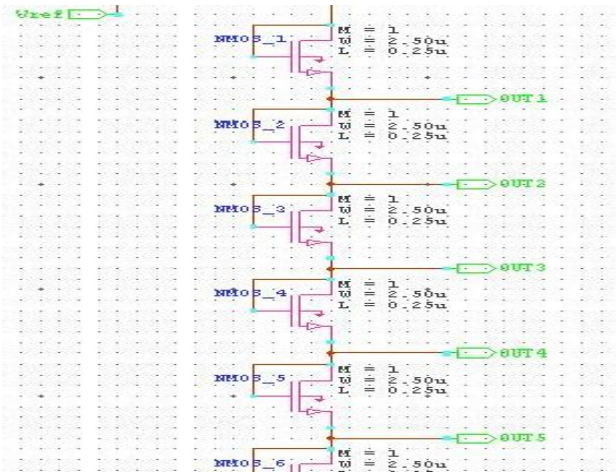

Fig.2 NMOS Resistor Ladder

III. LATCHED-BASED COMPARATORS

A comparator is used to find whether a signal is greater or smaller than reference signal. Comparators are mostly used in A/D converter design. The fast speed and low power make them suitable for more applications. In this

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paper we are using Latched Comparator In this we use three stage CMOS latched.

Proposed comparator consists of mainly three parts; Preamplifier, pseudo dynamic latch and output buffer.

Fig.3 Block diagram of comparator

Comparators in which there are three stages of latched comparator are:

1. Preamplifier
2. Latch
3. Output Buffer

3.1 Preamplifier Design

Over drive recovery time of the comparator is a speed limiting factor in high speed analog-to-digital converters. When a large input is followed by opposite polarity input, a high value of overdrive recovery time is occurring. Adding an extra input CLK to this preamplifier structure reduces the comparator overdrive recovery time with excess power dissipation. In order to reduce the on resistance of the extra transistor, the W/L ratio is chosen as (360/100). Effectively it increases the speed of the comparator.

During CLK=1, the preamplifier amplifies the difference between the inputs and the outputs are available at the output nodes (VP and VM). When CLK=0, PMOS transistor is switched on and equalize the output nodes so that overdrive recovery time is reduced.

The W/L ratio is chosen in such a way that the gain of the preamplifier gives a value of 2.5. The propagation delay with and without the extra transistor are 180 ps and 200 ps respectively.

3.2 Modified current source architecture

MOSFET which is operating in saturation works as a constant current source. NMOS transistor connected to VDD acts as a constant current source in the preamplifier.

The disadvantage of this current source is that through gate source capacitance, a short circuit can happen between VDD and ground. In order to avoid this, modified current source architecture is introduced with the use of current mirror scheme. By adjusting the (W/L) value of M5 and keeping the (W/L) of M7 and M8 same, the identical value of drain current can be obtained what it is getting in the first case.

This method is having the advantage of eliminating the direct path from VDD to ground through gate source capacitance thereby introducing more safe operation of the circuit.

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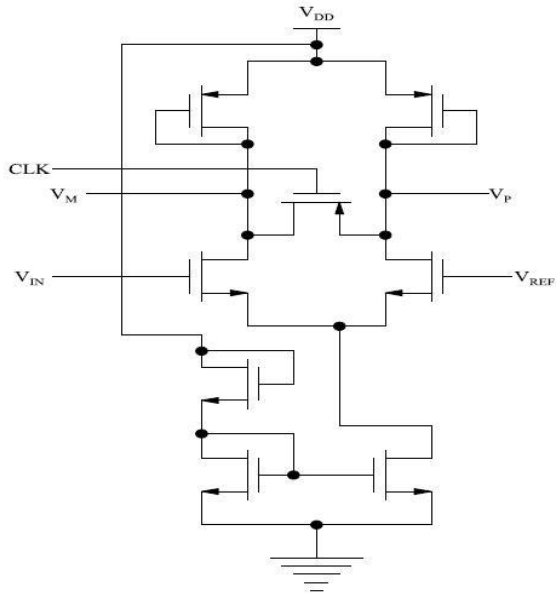

Fig.4 Preamplifier Design

3.3 Proposed pseudo dynamic latch

When clock is low, the latch is working in regenerate mode. Compared with dynamic latch, one NMOS pull down transistor which is connected to clock is removed in the pseudo dynamic latch.

The switching transistor is used to short circuit the latch's differential nodes to a common DC level. Increasing the width of the transistor brings the DC level on both sides near to each other.

To make the reset operation fast, the (W/L) of M13 should be taken as (360/100). Effectively it increases the speed of the latch by decreasing the pull down path delay in comparison with the dynamic comparator. In order to maintain the proper working of the circuit, the size of PMOS and NMOS transistors must be chosen carefully.

The disadvantage of pseudo dynamic latched comparator is the presence of static power dissipation. When clock is low, current flows from VDD to ground (pull up as well as pull down path is on), that gives rise to an extra power dissipation called static power dissipation which is not present in dynamic comparators. So with the help of pseudo dynamic logic, speed of the latch is increased with an added amount of static power dissipation. When clock is high, latch is operating in reset mode and the regenerating output nodes are at a voltage VDD/2.

The propagation delay with pseudo dynamic latch is 148 ps, which is a very less value as compared with dynamic logic.

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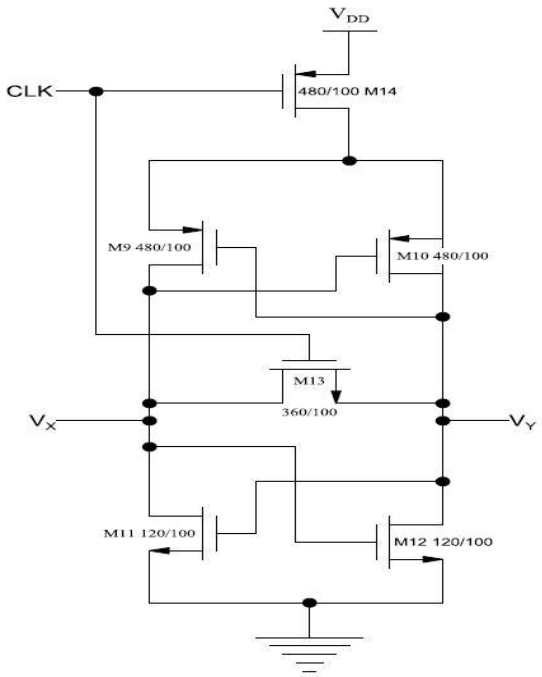

Fig. 5 Dynamic Latch

3.4 Output buffer

The function of the output buffer is to convert the latch output into logic high or logic low level value. The circuit consists of two parts.

Self biased differential amplifier and two inverters. Conventional CMOS differential amplifiers which are operating in saturation region cannot provide the switching current that is higher than quiescent current which is set by the current source device.

The ability of providing momentarily high current pulses helps the self biased differential amplifier suitable for high speed comparator applications. The differential amplifiers are complimentary to each other. The n-type devices works in a push-pull style with a matching p-type device. With the help of negative feedback, the differential amplifiers are self biased.

The advantage of this is that active region biasing is having less sensitivity towards variations in temperature, processing and supply. When VX = 1 and VY= 0, node potential at X goes down which makes the output node to be charged to VDD through a path shown in Fig. 9.

In the similar way when VX = 0, VY = 1, node potential at X goes up which makes the output node to be discharged to ground through a path.

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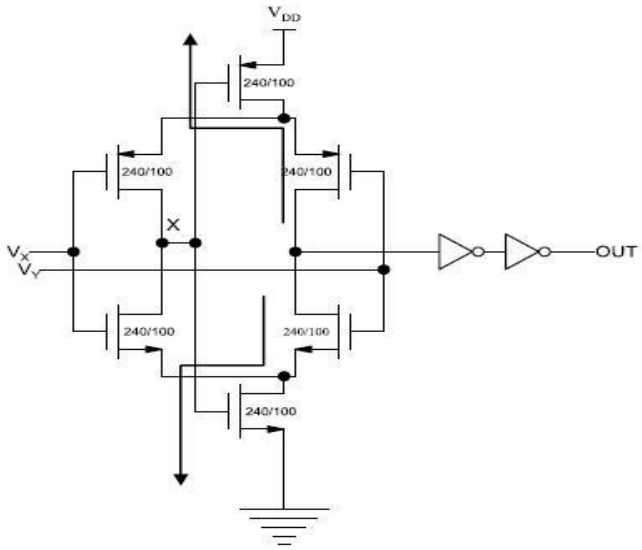


Fig.6 Output Buffer

IV. RESULTS

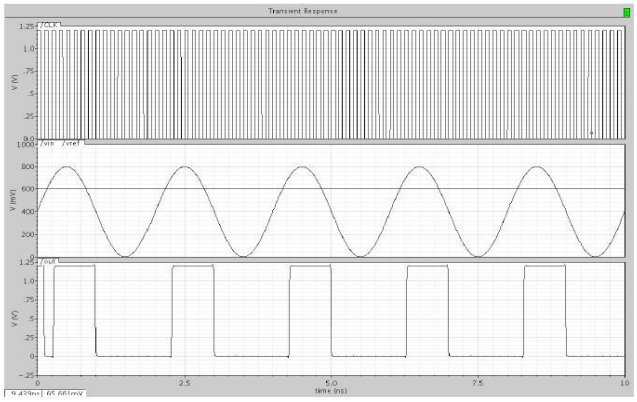
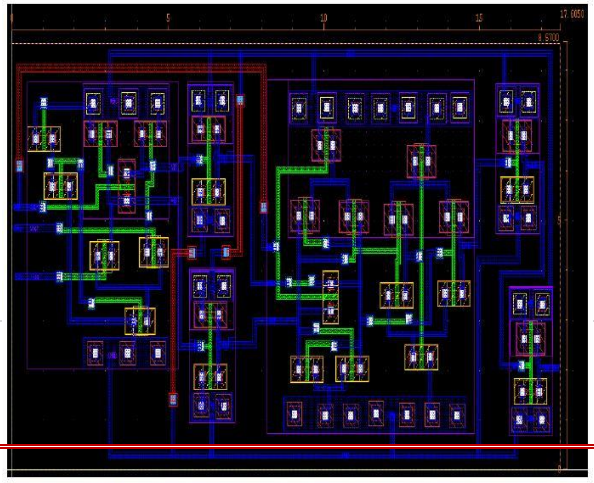


Fig.7 Comparator Result



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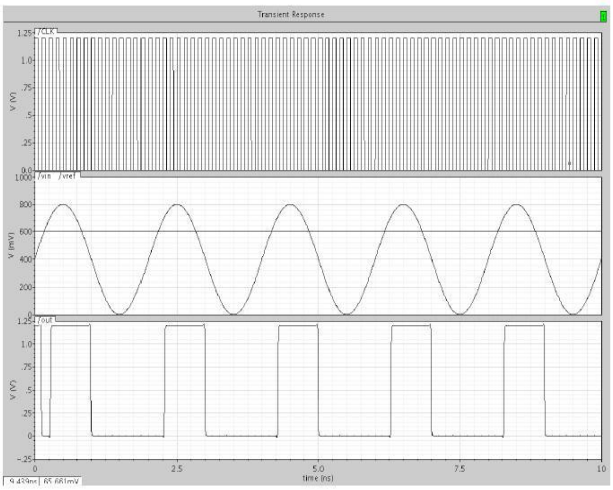
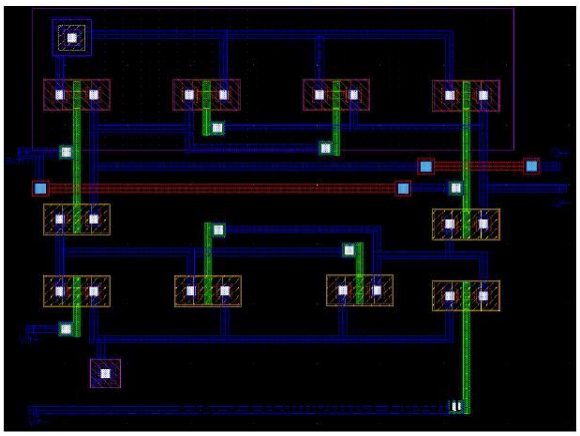


Fig. 8Comparator Layout



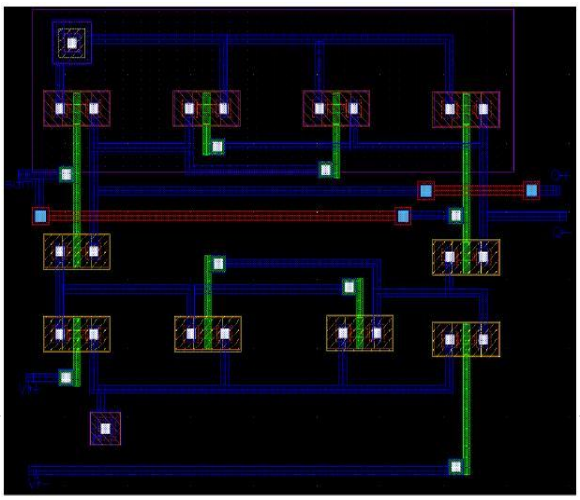


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Fig. 10 Dynamic Latch Layout

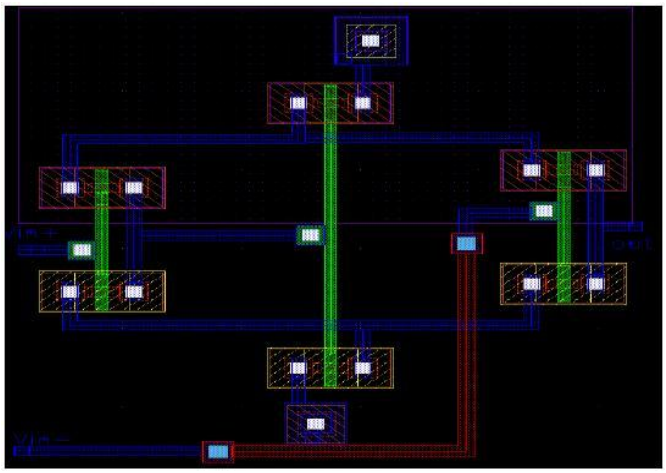

Fig. 11 Output Buffer Layout

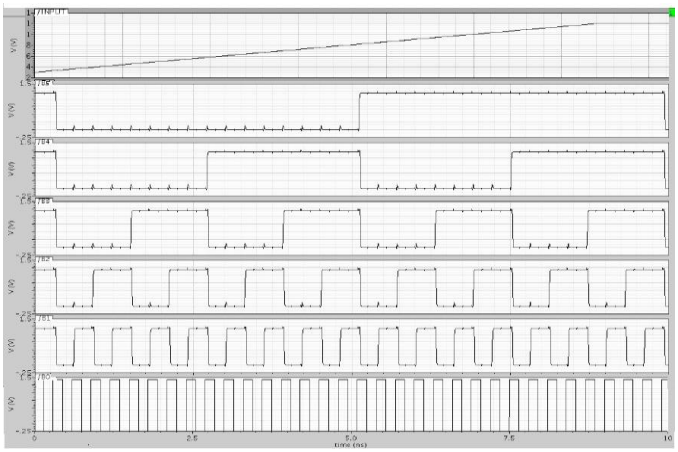

Fig. 12 Output of 6-bit Flash ADC

V. RESULT SUMMARY

Table.1

References	Proposed	Existing[1]	Existing[2]
Technology	45 nm	180 nm	90 nm
Architecture	Flash	Flash	Flash
Resolution	6-bit	5-bit	5-bit
Sampling Freq.(GS/s)	5 GHz	5 GHz	5 GHz
Supply Voltage	±O. 5 V to 2.5 V	±O. 5 V	1. 2 V
Power	0.68µW	23. 29µW	0.3149mW

VI. CONCLUSION

The design is simulated using TANNER-EDA tool. The threshold voltage levels for 6-bit Flash ADC using 45nm technology have been presented using TANNER- EDA tools. The power supply voltage given is 1.5 V. The challenges in designing high-speed CMOS flash ADCs are optimizing the speed and power, static and dynamic offset reduction, calibration, and low supply voltage operation. The results for comparators of 6-bit Flash ADC are tabulated in Table 1.Flash ADC circuits offer higher speed rates while maintaining a comparable power consumption level. The NMOS Resistor ladder, latched-based comparators, buffer and encode technique is used for to reduce power, increased speed & small size.

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