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FPGA implementation of basic adder circuits using reversible logic gates

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ABSTRACT

An addition or summing is a fundamental arithmetic operation which is used extensively in many very large-scale integration (VLSI) chips such as application-specific digital signal processing (DSP) and microprocessors chips. An adder determines the overall performance of the circuits in most of those systems. This paper proposes novel designs of basic adders using reversible logic gates. Reversible logic has become one of the most promising research areas in the past few decades and has found its applications in several technologies; such as low power CMOS, nano-computing and optical computing. Reversible logic gates are widely known to be compatible with future computing technologies which virtually dissipate zero heat low power dissipation.

Adders are fundamental building blocks in many computational units. For this reason, various adder topologies with reversible logic are designed using VHDL targeting XILINX's Spartan 3E FPGA board and delays are compared with conventional gate designs.

Keywords: Adder, FPGA , Garbage outputs, low power dissipation, reversible logic, VHDL.

I. INTRODUCTION

In electronics, an adder or summer is a digital circuit that performs addition of two numbers, which is used in many arithmetic logic units (ALU), floating-point units of processors and in many digital signal processing architectures. Adders are used not only in the arithmetic logic unit, but also in other parts of the processors, for address generation in the case of cache or memory Access.

II. INTRODUCTION TO REVERSIBLE LOGIC

Reversible logic has become one of the promising research directions in low power dissipating circuit design in the past few years and has found its applications in low power CMOS design, cryptography, optical information processing and nanotechnology [1]. Power dissipation is one of the most important factors in VLSI circuit design. Irreversible logic circuits dissipates $kT.\log_2$ Joule (k is the Boltzmann constant and T is the absolute temperature) heat for every bit of information that is lost irrespective of their implementation technologies [2].

Information is lost when the input vectors cannot be recovered from circuit's output vectors. Reversible logic naturally takes care of heating since in reversible circuits the input vectors can be uniquely recovered from its corresponding output vectors. Bennett showed that zero energy dissipation is possible only if the gating network consists of reversible gates [4].Thus reversibility will become future trends towards low power dissipating

circuit design. Reversible logic design differs significantly from traditional combinational logic design approaches.

A circuit (gate) is reversible if there is a one-to-one correspondence between the inputs and the outputs. Thus, any reversible gate has the same number of input and output lines, and it implements a permutation from input values to output values. Neither feedback nor fan out is allowed in reversible logic. Consequently, synthesis of reversible logic is different from irreversible logic synthesis. One of the major constraints in reversible logic is to minimize the number of reversible gates used and garbage outputs produced.

A logic synthesis technique using reversible gate should have the following features:

- Use minimum number of garbage outputs
- Use minimum input constants
- Keep the length of cascading gates minimum
- Use minimum number of gates

Reversible logic supports the process of running the system both forward and backward. This means that reversible computations can generate inputs from outputs and can stop and go back to any point in the computation history. Thus, reversible logic circuits offer an alternative that allows computation with arbitrarily small energy dissipation. Furthermore, reversible circuits are of major interest in optical computing, low power design, quantum computing and nanotechnology based systems. It is not possible to realize quantum computing without reversible logic. Reversible computation in a system can be performed if the system is composed of reversible gates.

Loss of energy is an important consideration in digital design. Part of the problem of energy dissipation is related to non-identity of switches and materials. Higher level of integration and the use of new fabrication processes have dramatically reduced the heat loss over the last decades. The design that doesn't resulting information loss called reversible.

III. REVERSIBLE LOGIC GATES

3.1 Basic Reversible Logic Gates

Reversible logic gates are very much in demand for the future computing technologies as they are known to produce zero power dissipation under ideal conditions. A reversible circuit can be realized by using reversible gates only. Reversible logic imposes many design constraints that need to be either ensured or optimized for implementing any particular Boolean functions. Though it is already described briefly about garbage outputs, this section can be defined with more appropriate examples and figures to describe all about reversible logic and reversible logic gates.

Garbage is the number of outputs added to make an n-input k-output Boolean function ((*n*, *k*) function) reversible. In other sense, a reversible logic gate has an equal number of inputs and outputs (*kXk*) and all the outputs are not expected. Some of the outputs should be considered to make the circuit reversible and those unwanted outputs are known as garbage outputs. A heavy price is paid for every garbage outputs.

3.1.1 FEYNMAN Gate

The most well known (2, 2) reversible gate is the Feynman gate. The logical functions performed by a Feynman gate with input vector (A, B) and output vector (P, Q) are shown in Fig.3.1. In Feynman gate, one of the input

bits act as control signal (A). That is, if A= 0 then the output Q follows the input B. If A = 1 then the input B is flipped at the output Q. So it is called as controlled NOT (1-NOT) and also called as quantum XOR because of its popularity in the field of quantum computing. This gate is one-through gate which means that one input variable is also output. Feynman gate acts as copying gate when the second input is zero by duplicating the first input at the output.

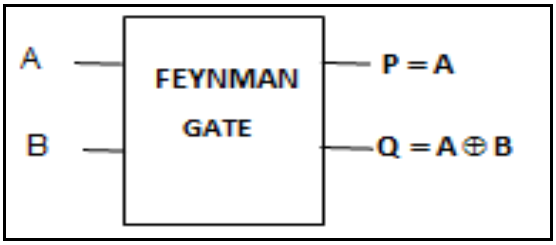

Fig 3.1: Feynman Gate

3.1.2 FREDKIN Gate

Fredkin gate, shown in Fig.3.2, is a (3, 3) reversible gate which realizes P=A, Q=A'B⊕AC and R=A'C⊕AB where (A, B, C) is the input vector and (P, Q, R) is the output vector. Fredkin gate is also self-reversible as it is its own inverse. It is a conservative gate because the hamming weight (number of logical ones) of an input is same as its output. It uses 'A' as its control input if A = 0, then the outputs are simply duplicates of the inputs; otherwise if A = 1, then the two input lines (B and C) is interchanged at the output. Fredkin gate is a universal gate, that is, we can construct the basic blocks such as AND, OR, NOT and other gates from this Fredkin gate by pre-setting some of its inputs.

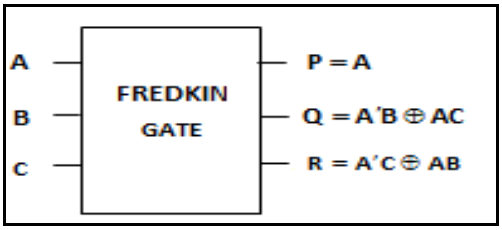

Fig 3.2: Fredkin Gate

3.1.3 TOFFOLLI Gate

Tofolli gate is one of the example for (3, 3) reversible gates. Fig. 3.3 shows the Tofolli gate. This gate is two through gate because two of its outputs are identical with its inputs. Because of this, Tofolli gate is also known as two controlled NOT (2-CNOT). If the first two input bits are one, then the third output bit is the inverse of third input bit i.e., A = B = 1, then R = C. Tofolli gate performs basic AND operation when zero is given as its third input (C = 0; R = AB). Any reversible gate has an inverse or dual. The dual of Tofolli gate is also a Tofolli gate and so it is self-reversible.

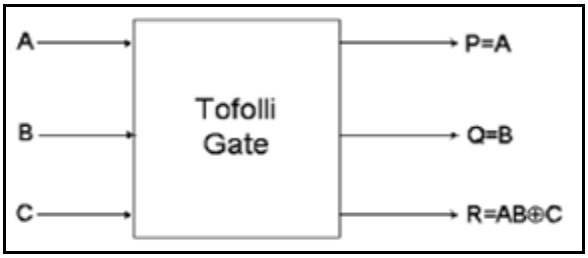

Fig: 3.3 Toffoli gate

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3.1.4 PERES Gate

Peres gate is another important gate which has a low quantum cost as compared to other gates. It is shown in Fig.3.4. A single Peres gate can give generate and propagate outputs when the third input C = 0. Because of this, it is quite useful while designing carry look-ahead adders.

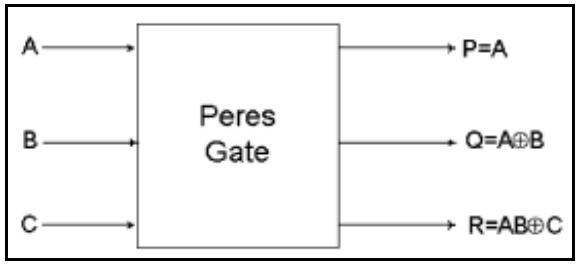

Fig: 3.4 Peres Gate

3.1.5 NEW Gate

The new gate shown in Fig.3.5 is another gate which implements all the basic operations like a universal gate.

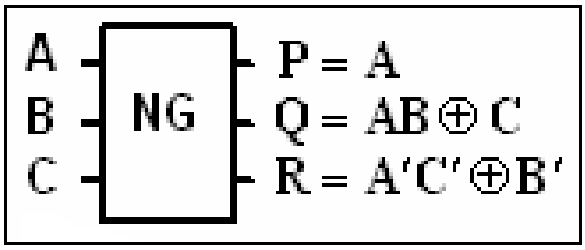

Fig: 3.5 New Gate

3.1.6 DOUBLE FEYNMAN Gate

The Double Feynman gate shown in Fig.3.6 is another gate which is also used to implement all basic operations.

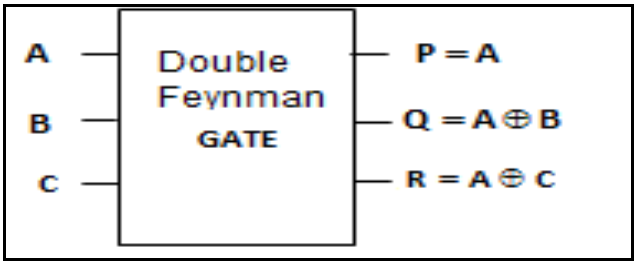

Fig: 3.6 Double Feynman Gate

3.1.7 NEW TOFOLLI Gate

A 3X3 New Tofolli Gate (NTG) can be defined as I_v = (A, B, C) and O_v= (P=A, Q= A ⊕ B, R=AB ⊕C) where I_v and O_v are the input and output vector respectively. Fig. 3.7 shows the block diagram of 3X3 New Tofolli Gate (NTG).

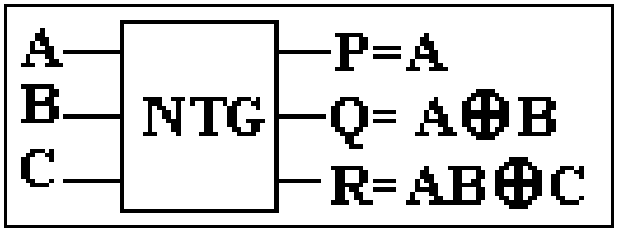

Fig: 3.7 3X3 New Toffoli Gate

3.1.8 TSG Gate

A 4 X 4 one through reversible gate called TS gate "TSG" is developed. The reversible TSG gate is shown in Fig. 3.8. The TSG gate can implement all Boolean functions. One of the prominent functionality of the TSG gate is that it can work singly as a reversible Full adder unit.

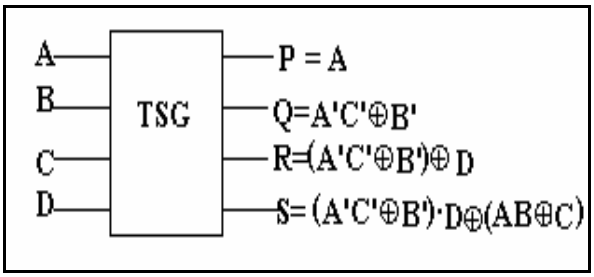

Fig: 3.8 Reversible 4 X4 TSG Gate

3.1.9 HNG Gate

A 4 X 4 PG gate is a universal gate. Where Iv and Ov are the input and output vectors. The HNG gate is shown in Fig. 3.9, where each output is annotated with the corresponding logic expression. One of the prominent functionalities of the HNG gate is that it can work singly as a reversible full adder unit. If Iv = (A, B, Cin, D), then the output vector becomes: Ov= (P=A, Q=B, R= A⊕B⊕C, S= (A⊕B).C⊕AB⊕D).

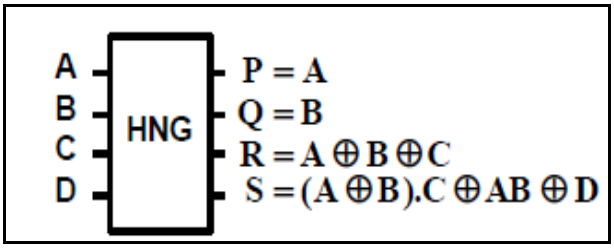

Fig: 3.9 Reversible 4x4 HNG Gate

3.1.11 DPG Gate

4*4 DPG gate is a combination of two 3x3 PERES GATE. As we know that the Peres Gate has a low quantum cost as compared to other gates, so the combination of it provide more useful Double Peres Gate. This gate can singly work as many combinational circuits as FULL ADDER & FULL SUBTRACTOR This gate requires only one clock cycle and produces no extra garbage outputs, that is, it adheres to the theoretical minimum as established

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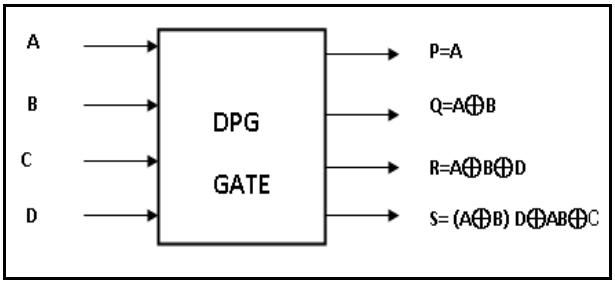

Fig: 3.10 Reversible 4x4 DPG Gate

IV. HARD WARE IMPLEMENTATION

The hardware model of the adders are designed by targeting XILINX's Spartan 3E FPGA board and simulations where performed using Xilinx in built ISE simulator. For implementation VHDL programming language is used. In this work basic adders like ripple carry adder, carry select adder and carry look ahead adder are designed using reversible logic gates.

V. SIMULATION RESULTS

The functionality of hardware model is verified by the process called simulation. Here the simulation of the model is done by ISE Simulator.

5.1 Half Adder

Figure 5.1 shows the simulation results of half adder for the inputs a=1,and b=0.

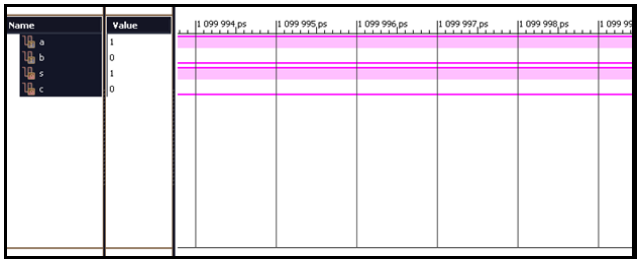

Fig: 5.1 simulation results of half adder

5.2 Full Adder

Figure 5.2 shows the simulation results of full adder for the inputs a1=1,b1=1, and c1=1.

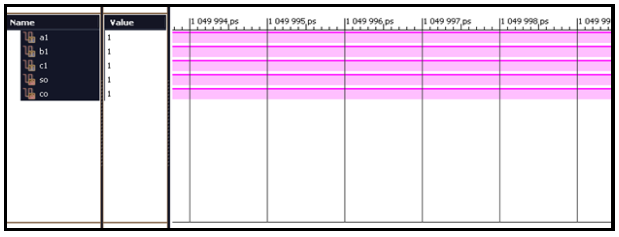

Fig: 5.2 simulation results of full adder

5.3 Ripple Carry Adder(Rca)

Figure 5.3 shows the simulation results of ripple carry adder for the inputs ar=1111, and br=1100.

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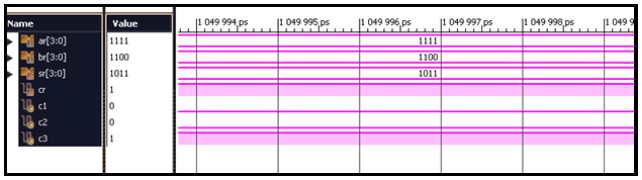

Fig: 5.3 simulation results of ripple carry adder

5.4 Ripple Carry Adder With Reversible Logic Gates

Figure 5.4 shows the simulation results of ripple carry adder with reversible logic for the inputs ar=1111,br=1100,and cin=1;

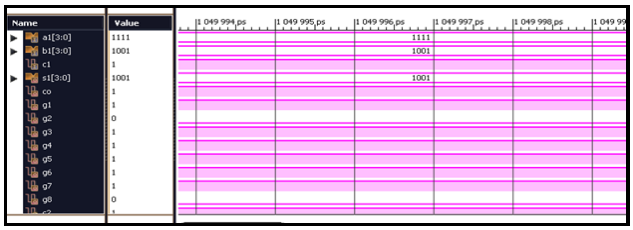

Fig: 5.4 simulation results of ripple carry adder

5.5 Carry Select Adder

Figure 5.5 shows the simulation results of carry select adder for the inputs ac=1111, bc=1001, and cin=1;

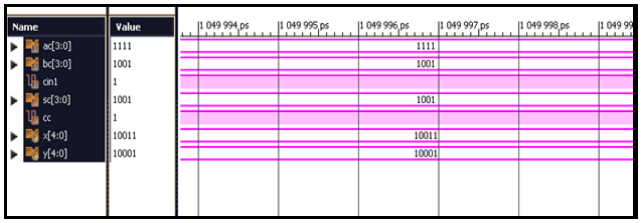

Fig: 5.5 simulation results of carry select adder

5.6 Carry Select Adder With Reversible Logic Gates

Figure 5.6 shows the simulation results of carry select adder with reversible gates.

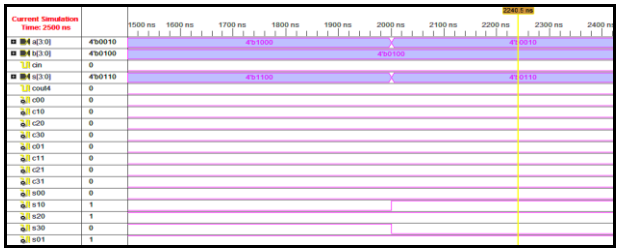

Fig: 5.6 simulation results of carry select adder with reversible logic

5.7 Carry Look Ahead Adder

Figure 5.7 shows the simulation results of carry look ahead adder for the inputs a=1111,b=1001,and cin=1;

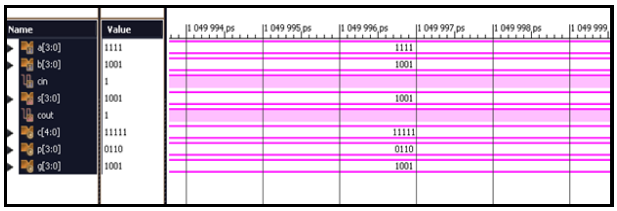

Fig: 5.7 simulation results of carry look ahead adder

5.8 Carry Look Ahead Adder With Reversible Logic Gates

Figure 5.7 shows the simulation results of carry look ahead adder in reversible logic for the inputs a=1111,b=1001,and cin=1.

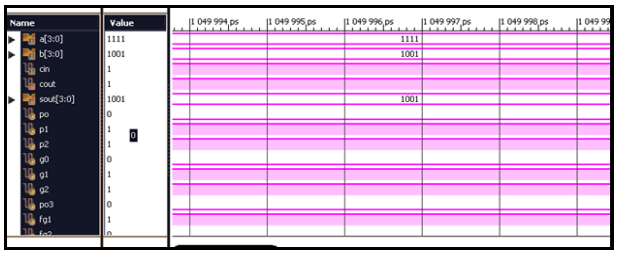

Fig: 5.8 simulation results of carry look ahead adder with reversible gates

VI. DELAY COMPARISION

Below Table 6.1 represents the delay comparison of various adder topologies in conventional logic and reversible logic.

Table 6.1 Delay comparison

Adder topology	Delay		Percentage of delay reduction in reversible logic
	Conventional gates	Reversible gates	
Ripple carry adder(RCA)	11.00sec	8.00sec	27.27%
Carry select adder(CSLA)	17.00sec	11.00sec	29.41%
Carry look ahead adder(CLA)	12.00	10.80sec	10.00%

VII. CONCLUSION

In this paper basic adders like ripple carry adder, carry select adder and carry look ahead adder are designed and analysed. The architecture is designed specially to make them suitable for reversible logic synthesis. The simulation and synthesis of these circuits has been done using XILINX Software. Delay comparison of various adder topologies in conventional logic and reversible logic is done. Reversible gates consume less power and produce less delay compared to conventional gates.

REFERENCES

[1] J. M. Rabaey, Digital Integrated Circuits—A Design Perspective. Upper Saddle River, NJ: Prentice-Hall, 2001.

[2] R.Landauer, "Irreversibility and Heat Generation in the Computational Process", IBM Journal of Research and Development, 5,pp. 183-191,1961.

[3] Dmitri Maslov, "Reversible logic synthesis", University of New Brunswick, September 2003.

[4] C.H.Bennett, "Logical Reversibility of Computation", IBM J. Research and Development, pp.525-532, November1973.

[5] Feynman R., 1985. Quantum mechanical computers, Optics News, 11:11-20.

[6] Toffoli T., 1980. Reversible computing, Tech Memo MIT/LCS/TM-151,MIT Lab for Computer Science.

[7] Fredkin E. and T. Toffoli, 1982. Conservative logic. Int'l J. Theoretical Physics, 21: 219-253.

[8] Azad Khan Md. M. H., 2002. Design of full adder with reversible gate. International Conference on Computer and Information Technology, Dhaka, Bangladesh, pp. 515-519.

[9] Peres, A. 1985. Reversible logic and quantum computers. Physical Review A, 32: 3266-3276.

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