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TEST BENCH FOR FAULT LOCATION IN ELECTRICAL POWER DISTRIBUTION SYSTEMS

M. Zahri[1], Y.Menchafou[2], M. Habibi[3], H. El Markhi[4]

[1,3]Laboratory of Telecommunication and Engineering Decision Systems, IbnTofail University, Kenitra, Morocco

[2,4]Laboratory of Signals, Systems and components, Sidi Mohamed Ben Abdellah University, Fez, Morocco

ABSTRACT

Accurate Fault location in an Electric Power Distribution System (EPDS) is important in maintaining system reliability. Several methods have been proposed in the past. However, these methods present a conceptual studies and algorithms of fault location trying to find a simple and reliable fault location algorithm.Their implementation requires having several parameters, as the network data and the voltages and currents before and during the fault, these parameters can be obtained only by using an acquisition and processing system. In this paper, we present a test bench for the display, storage and use of currents and voltages before and during a fault occurring on an electric power distribution system in order to use them in the fault location algorithms. The test results are achieved from the real test of the test benchusing a part of a low voltage network simulating a fault on a three-phase cable that powers resistive loads.

Index Terms:Test Bench, Electric Power Distribution Systems, Fault Location, Electronic Processing Card.

I. INTRODUCTION

Distribution networks are dispersed in each urban and rural region, and are crossed from each alley and street. Each distribution feeder has many laterals, sub-laterals, load taps, balanced and unbalanced load and different types of conductors [1]. Power distribution systems (PDSs) are subjected tofault conditions caused by various sources such as adverse weather conditions, equipment failureand external object contacts. Nevertheless, Owing to the expansion of distribution networks, to their radial topology and to the existence of short and heterogeneous lines and of intermediate loads, it is very difficult and complicated to locate the fault in these networks.

Currently the only technique used for locating faults in distribution systems of electric poweris the visual inspection of FPI (Fault Passage Indicators) which imposes an important time of restoration..

In the past, various fault location algorithms have been developed. Novosel et al. (1998) make use of apparent impedance, defined as the ratio of selected voltage to current based on fault type and faulted phases, to locate faults in [2]. In [3], Das (1998) locates the faulted section and next the distance to the fault in this section is calculated. Yang and Springs (1998) propose a fault location method which corrects the fault resistance effects in [4]. The method proposed by Das et al. (2000) in [5] used the fundamental frequency voltages and currents

measured at a line terminal before and during the fault. In [6] the method proposed by Saha and Rosolowski (2002) estimates the fault location by comparing the measured impedance with the calculate feeder impedance assuming faults each section line. Choi et al. (2004) locating faults by solving a quadratic equation resulting from the direct circuit analysisin [7]. Senger et al. (2005) in [8] proposed a method that it was based on measurement provided by intelligent electronics Devices (IEDs). In [9] Kim et al. (2007) estimated fault location on distribution feeders using Power Quality monitoring data. A way to optimally place faulted circuit indicators along the feeder is developed in [10] by Almeida et al. (2011). Methods to reduce and eliminate the uncertainty about the fault location are discussed by authors of [11, 12] (2012). In [13], Sadeh et al. (2013) suggested a new algorithm for radial distribution systems using modal analysis. Wanjing et al. presented a novel method based on two types of fault location approaches using line to neutral or line to line measurement at substation in [14] (2014). In [15], Zahri et al. (2014) proposed a new hybrid method based on ANN and Apparent impedance calculation to determinate the Faulty section of line. A reduced algorithm for fault location in EPDS is suggested by Zahri et al, in [16] (2015).

According to literature review, these methods present a conceptual studies and algorithms of fault location trying to find a simple and reliable fault location algorithm, before being implemented on data processing systems for the practical use.

These algorithms are generally based on impedances computation; their implementation requires having several parameters, as the network data and the voltages and currents before and during the fault, these parameters can be obtained only by using an acquisition and processing system.

In this paper, we present a test bench for the display, storage and use of currents and voltages before and during a fault occurring on an electric power distribution system in order to use them in the fault location algorithms, considering that the stages of acquisition and conditioning of these currents and voltages were made before.

The remainder of this paper is organized as follows: The Fault Location Procedure and the Proposed Test Benchare presented in sections II and III respectively, the test results are shown in Section IV, whereas the conclusions of this work are presented in Section V.

II. FAULT LOCATION PROCEDURE

2.1 Fault Location Steps

The supply of electricity, in terms of safety and availability, is a key point in the management of electricity grids, when distribution system outages occur, speedy and precise fault location is crucial in accelerating system restoration, reducing outage time and significantly improving system reliability, and thus improving the quality of services and customer satisfaction. Fault location is then the most important task of network management. In general there are three levels of treatment following the occurrence of a fault in a distribution network:

Fault Detection: must be very fast because it will open the circuit breakers in order to put off the faulty part of the network. It is made from locally available information of Fault Passage Indicators (FPI) and protective relay (currents and voltages measurement).

Fault Location: can isolate the faulted zone (faulty sections) by the network reconfiguration. The fault location can be slower than the detection. However, it must be more precise in order to operate optimally the network switches. Nevertheless, we must not overlook that a slow location may delay replenishment of the clients, and affect the quality of service by increasing the not distributed energy.

Fault searching: is to calculate more accurately the distance between the fault point and a reference point of the line often represented by the bus-bar output from the source station.

These last two steps are merged by the current researches in the area of fault location to have an accurate and a real time fault location, which requires data before and during the fault in contrast to what is present in existing relays.

2.2 Data Processing Procedure for Fault Location

For protection in the existing protection systems, and for fault location in the target systems, it is necessary to process the data available on the network, such as the parameters of lines and voltages and currents before and during the fault, in order to reach that, the following procedure is necessary:

Figure.1. Data Processing Procedure for Fault Location in EPDS

Data Acquisition: Data acquisition is done mainly by voltage and current sensors, which are usually voltage and current transformers allowing having the image in the secondary of the physical magnitude to be measured available on the primary.

Signals Conditioning: This step allows adapting the level of the signal from the sensor to the processing system.

Signals Processing: The signal Processing is the steps including the following stages:

- Filtering
- Sampling
- Analog to Digital Conversion (ADC).

In order to have the output in different forms (display, storage, graphics and figures...).

III. THE PROPOSED TEST BENCH

After the acquisition and the conditioning of the voltages and currents from the distribution line, and in order to have the output in different forms (display, storage, graphics and figures...), the following processing card is proposed

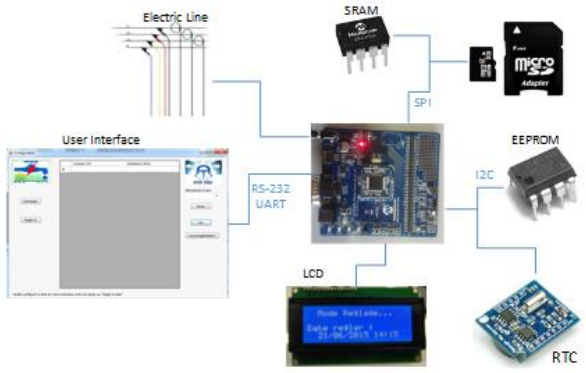

Figure.2. Block Diagram of the Proposed Relay

It is a DsPICDEM motherboard that embeds all the modules required for operating the DSP Such as voltage regulators, UART and its adapter, Switch's and the connector to simplify access to the DSP pins. It can receive many DsPIC including the DsPIC33F which will then be the heart of the proposed relay.

The DsPIC33F embeds several useful modules for our relay:

- Analog to Digital Converters (ADC)
- Direct Memory Access (DMA)
- Bus SPI
- Bus I2C
- Bus UART

The operation and characteristics of these modules will be discussed in detail subsequently.

3.1 Data conversion

It is the first element of the processing chain. After the acquisition of the six signals (I_1, I_2, I_3, V_1, V_2 and V_3) and their conditioning and filtering, they are transmitted to the ADC to convert them to digital values. To achieve that, the six analog inputs of DsPIC (AN4, AN5, AN12, AN13, AN14 and AN15) are scanned successively and repetitively, each scan is followed by two important steps that are the sampling and quantization (Conversion) as presented in the figure.3:

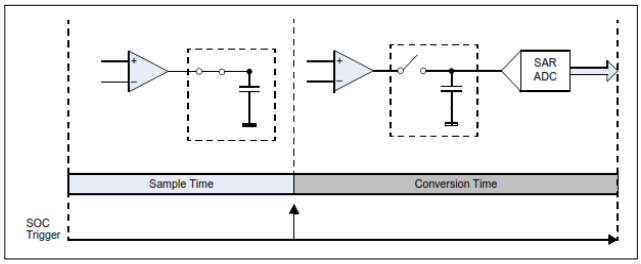

Figure.3. Data Conversion Steps

3.2 Data Storage

The addition of SRAM's in our processing card was not a choice, but an obligation. After studying the different blocks of DSP33F, we noticed that its internal RAM does not exceed 30K.

The SRAM's are used to store the data stack to make them available in case of fault.

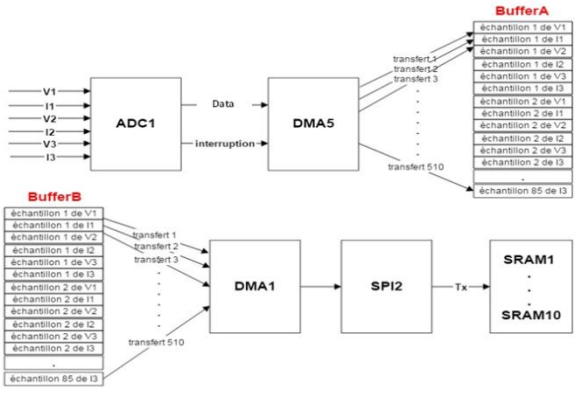

Figure.4.Data Storage Steps

Furthermore, in order to store the network and the fault database, the selection of the EEPROM was essential because of their ability to store data off, their simplicity of use and availability in the market.

3.3 Data Display

The LCD (liquid-crystal display) shows the human-machine interface in the relay, it displays the RMS values of currents and voltages, and indicates the presence of faults and relay status:

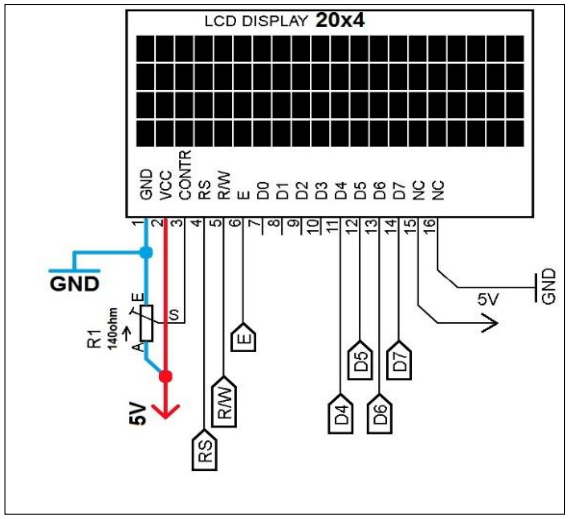

Figure.5 LCD Pins

3.4 Data Acquisition after Processing

After treatment of acquired physical quantities, parameters are essential to be used in fault location algorithms as mentioned in the figure.6, these data are:

- RMS signals.
- Phase shifts current-voltages.

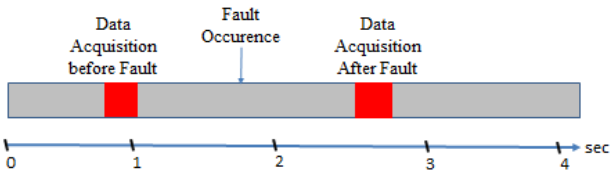

Figure.6.Voltages and Currents Acquisition After Data Processing

3.5 Data Storage on SD-Card

For more flexibility and to use all the samples placed in the SRAM's after the appearance of fault in other treatment systems such as PCs or software calculation or tracing. It was essential to add the SD card storage option as illustrated in the figure.7. This adding was a challenge because of the lack of the USB protocol in the dsPIC33F card and of the very low speed of UART Bus 11Kbit / s.

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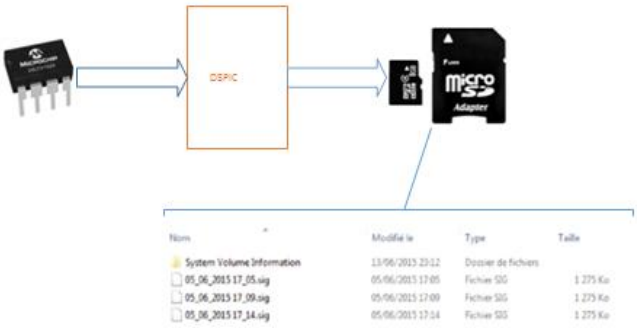

Figure.7.Data Storage on SD-Card

3.6 User Interface

To facilitate the configuration of the relay, display signal curves stored in the SD card and turned them into a Matlab file, we realized a software interface with the C# programming language.

This user interface presented in figure.8, consists of two windows, one for the configuration, it connects with the DsPIC via UART bus to record the network architecture or retrieve the existing one, it also sets the RTC or the synchronization module, the other window is for displaying the signals of currents and voltages.

Figure.8. User Interface

IV. TESTS AND RESULTS

The verification of the effectiveness of the proposed test bench consists first to realize the processing electronic card that assembles all the elements presented above, and then check its reliability on a practical case of fault.

4.1 The Electronic Card

To assemble the cards made in our work, we have designed an electronic card that contains the parts described above

This achievement is divided into two stages: □

- Design the artwork

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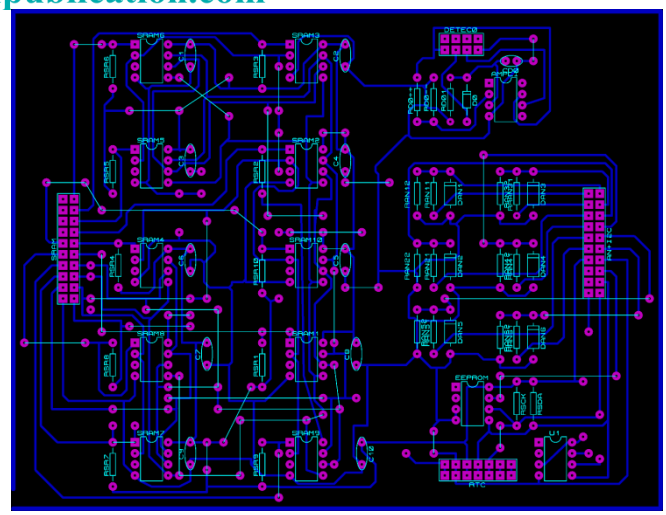

Figure.9. the Artwork of the Global Card

- Realization of the circuit

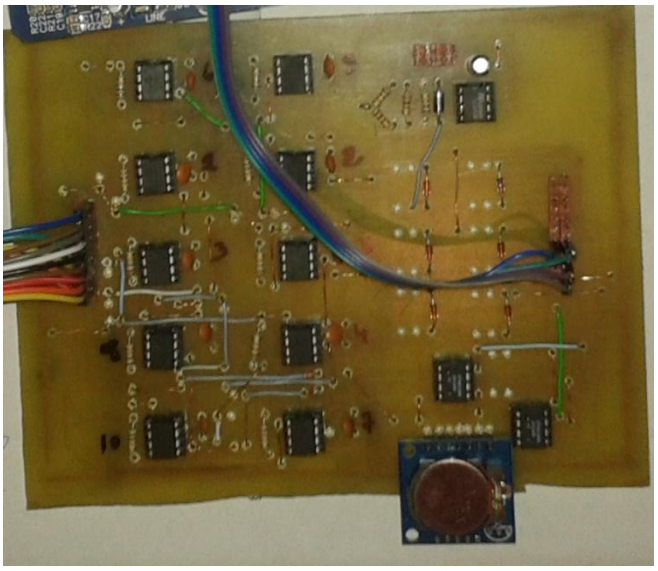

Figure.10. the Circuit of the Global Card

The final prototype is then shown in the following figure

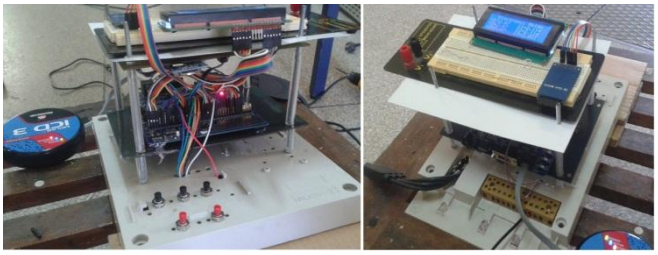

Figure.11. The Prototype of the Test Bench

4.2 System Simulated

The system studied, as shown in the figure.12, is a part of a low voltage network simulating a fault on a three-phase cable that powers resistive loads. The low voltage line is used because of the difficulty of making a test on a real Electric Power Distribution System.

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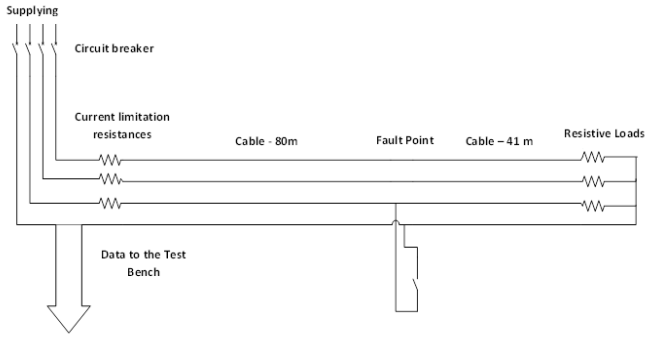

Figure.12. Simulated System.

4.3 Results

The test consists in feeding three resistive wye-connectedloads. Then, simulate a short circuit between phase and neutral and wait for the circuit breaker tripping. The test Bench (relay) detects the fault and records all six signals in the SD card.

Three tests were performed; their results were recorded on the SD card as illustrated on the figure.13:

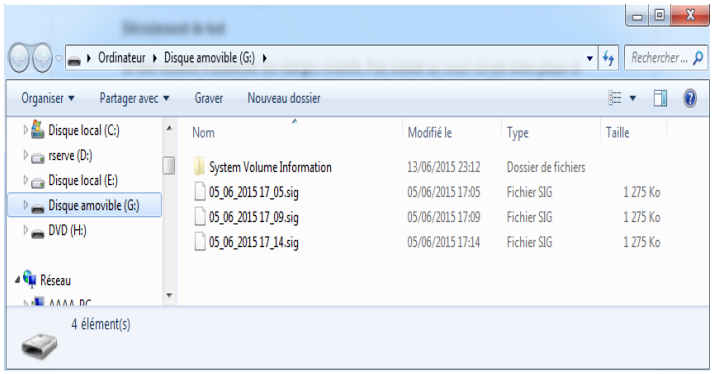

Figure.13. Test's Data Storage on SD Card

Then on the user interface, Currents and voltages curves before and during the fault are displayed as shown in Figure 14:

Figure.14. Displaying Test's Signals of Currents and Voltages

According to the figure.14, the three voltages and the three currents can be easily seen, before the fault, it is clear that the six values are normal. However after the fault, quantities become zero because of the opening of the circuit breaker of the faulty phase.

Therefore, the interface displays the fault current behavior on the curve I1, and also shows the good recording of the six signal values during the 4.2s, which includes the necessary information for the execution of the fault location algorithm.

V. CONCLUSION

A test bench to display, storage and use of currents and voltages before and during a fault occurring on an Electric Power Distribution System in order to use them in the fault location algorithms has been presented in this paper. It is based on a global electronic processing card including different operating modules such as ADC conversion, Data Storage and Display after the Data processing using a DsPIC33F. Most of the FL techniques found in the literature present a conceptual studies and algorithms of fault location trying to find a simple and reliable fault location algorithm, before being implemented on data processing systems for the practical use.

The performances of this prototype are verified by several tests simulating single line to ground fault cases ina part of a real low voltage network simulating a fault on a three-phase cable that powers resistive loads.

Test results show that the proposed fault location Test Bench is suitable to be used in EPDS thanks to its simplicity, its reliability and its robust effectiveness.

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