A LOW ENERGY, HIGH PERFORMANCE MULTIPLIER USING DM^2 ADDER

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ABSTRACT

This project presents a multiplier. This multiplier is designed using Dual Mode Square adder. The dual mode square adder has low energy dissipation also yield high performance. As it works in dual mode operation it works with less delay. Dual mode adder simplifies the usage of dual mode addition in a pipelined processor, while further reducing the computation energy compared to dual mode adder implementation, the proposed multiplier with dual mode square adder can achieve less area, high speed, less propagation delay time.

Key Words: DM^2, DMADD, DML,LSB,VHDL.

I. INTRODUCTION

The multiplier is designed in the way that it yields low energy and high performance. The design was implemented using the mixture of both behavioral design and rtl design. The multiplier has a controller to control the circuit. This controller circuit will command other modules. The multiplier circuit will multiply the value given by the multiplicand circuit. The dual mode square adder will perform the addition operation. This dual mode square adder is a combination of two technology *dual mode adder and dual mode logic.* The first method is *dual-mode addition* (DMADD). It takes advantage of the carry probability to perform low-power addition and leading to a considerable energy reduction of up to 50% compared to conventional designs. However, it requires some pipeline modifications to support multi-cycle addition. The second method is a logic gate topology called *dual mode logic* (DML) comprising static and dynamic operation modes within the same gate.

II. BLOCK DIAGRAM

The Multiplier is constructed using the essential parts in Fig1. It consists of controller, multiplicand, DM^2 adder and multiplier result. The controller is the heart of circuit that controls the circuit using the START and STOP Signal. Multiplier is generally preferred in Digital signal processing, CPU the Central Processing Unit. Multiplier with less area occupation and high delay is a challenging task. But the proposed method reduces the delay and increases the performance of Multiplier as the adder included is Dual Mode Square Adder. This DM^2 adder has high performance and less delay which in turn make the multiplier to achieve the required result.

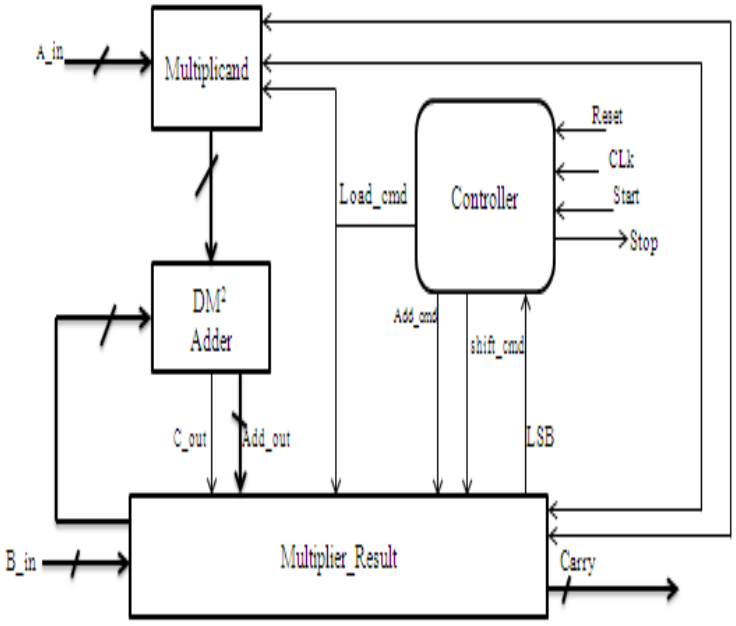

Fig 1. Block Diagram of Multiplier

The controller will receive the start signal then it will load the values in the multiplicand and multiplier result's shift register. The controller works by add and shift logic. The multiplicand and DM^2 adder will pass the value to multiplier result. Then the multiplied value will be achieved through the output from multiplier. The dual mode square adder works in two ways 8 bit Ripple Carry adder and two 4 bit carry select adder.

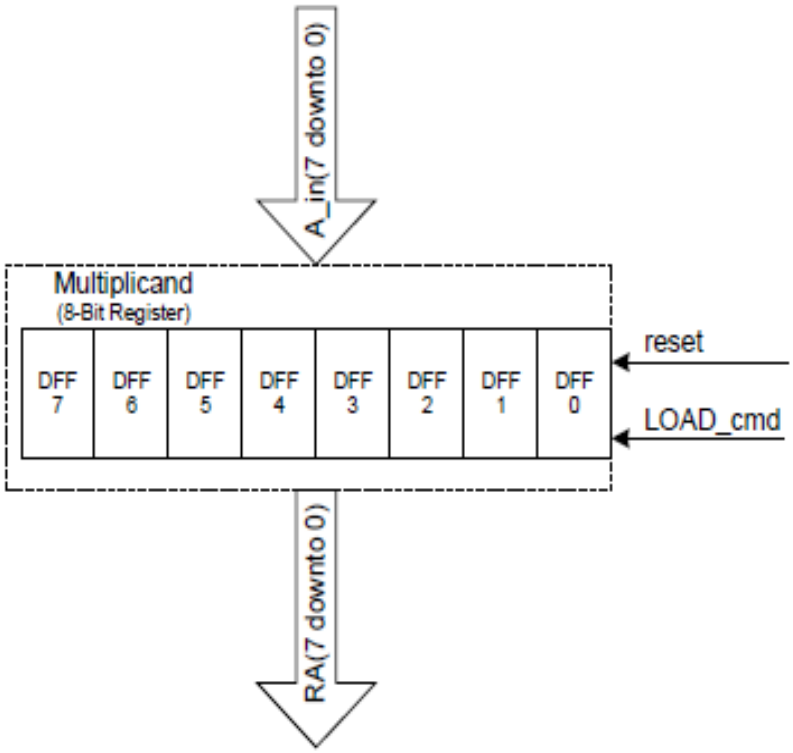

Fig 2 Multiplicand Block Diagram

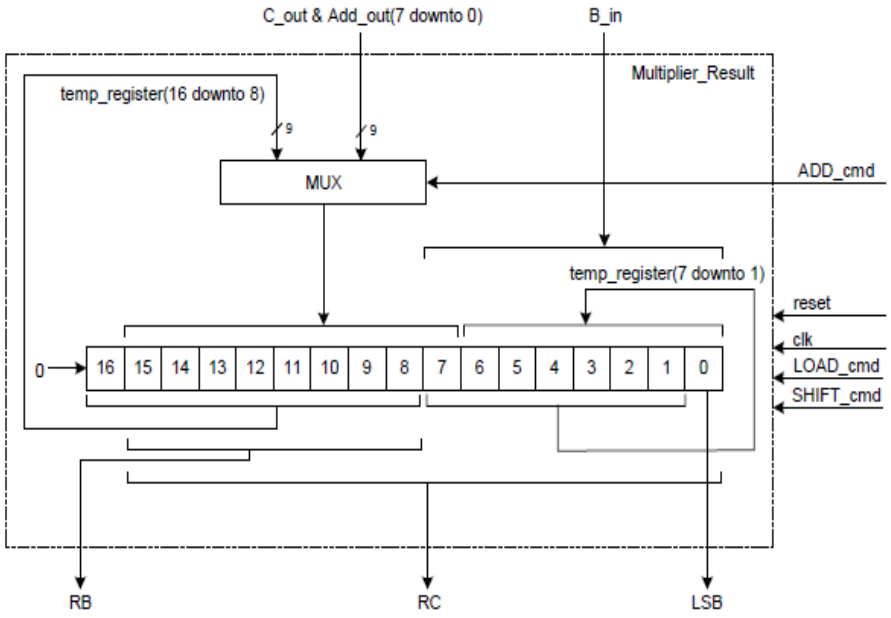

Fig 3 Multiplier Register

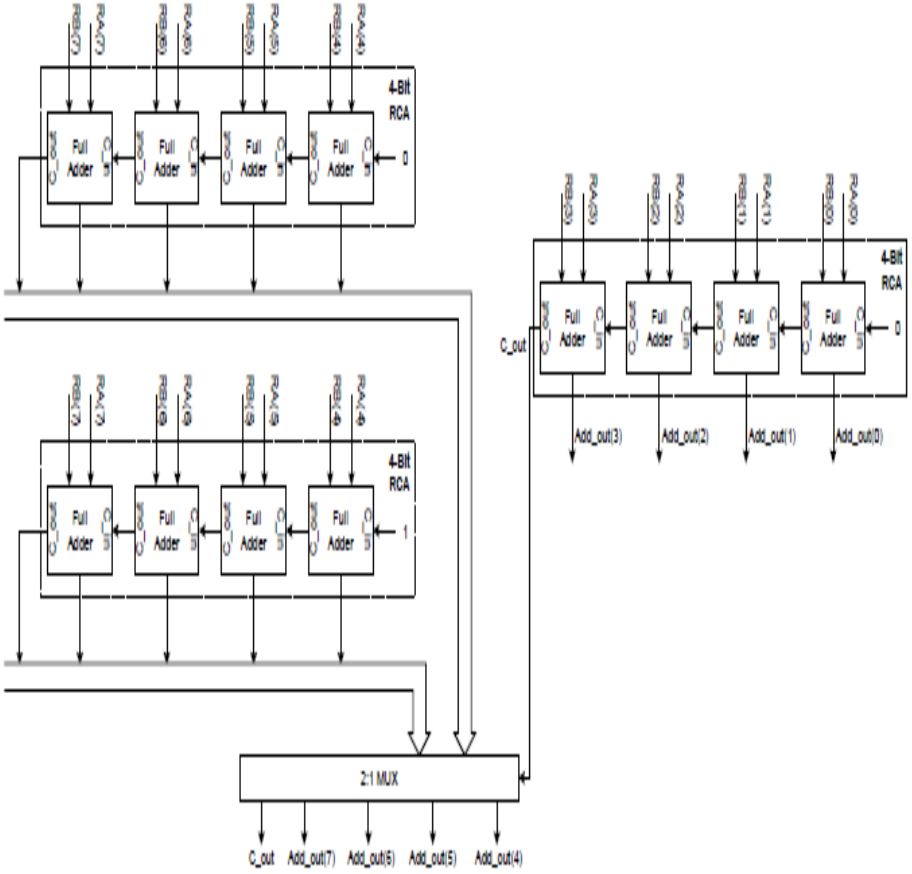

Fig 4 Carry Select Adder

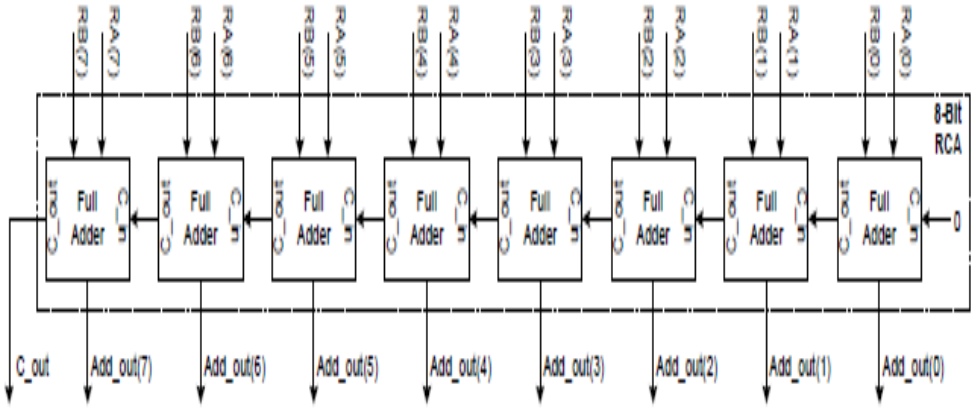

Fig: 5 Ripple Carry Adder

The 8-bit ripple carry adder is composed of 8 individual full adders connected in a chain. In this case, the carry out of each full adder is the carry in of the following full adder. The limiting speed factor in this approach is the delay from the first full adder to the outputs of the final full adder. In order to try and improve the speed of the adder, consequently enhancing the overall speed, the carry-select adder was also implemented and compared to the original ripple carry adder. The carry-select adder is composed of three 4-bit adder to its carry out which controls the ripple carry adder blocks whereby the carry out of the first ripple carry adder selects which of the other two ripple carry adders to send to the output. In this case the limiting factor is the delay from the input of the first 4-bit ripple-carry multiplexer.

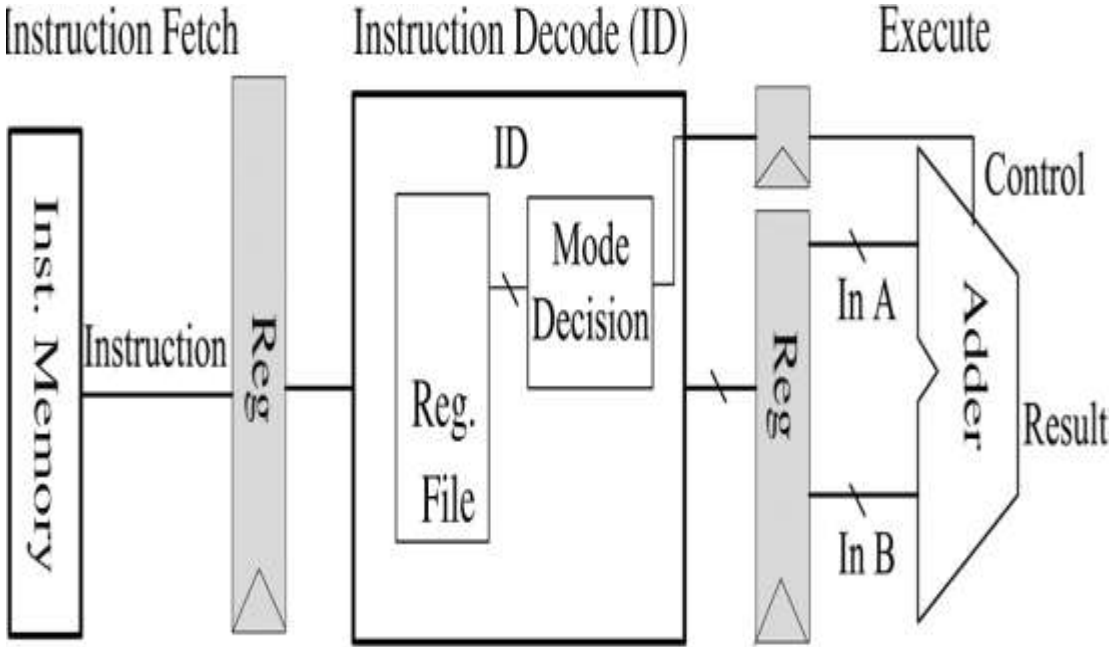

Fig.3 Dual Mode Square Adder

III. SIMULATION AND TIMING

The controller is synchronous to the clock and transitions through the various states occur on the rising clock edge. Upon entering the initialize state, the LOAD_cmd is generated. During each test state, the LSB is

sampled. If the LSB was high, the add state is entered and the controller generates the ADD_cmd. The input, A_in, is only loaded into the register on the rising edge of the LOAD_cmd signal and remains in the register until the next time the LOAD_cmd signal is asserted. If the Multiplier_Result receives a SHIFT_cmd without a prior ADD_cmd, the register will be shifted logically to the right. If the ADD_cmd precedes the SHIFT_cmd, bits 1 to 7 of the register will be placed into positions 0 to 6 while the 9 inputs bits from the adder will be placed into positions 7 to 15 of the register. This is essentially equivalent to storing the adder results and then shifting the entire register.

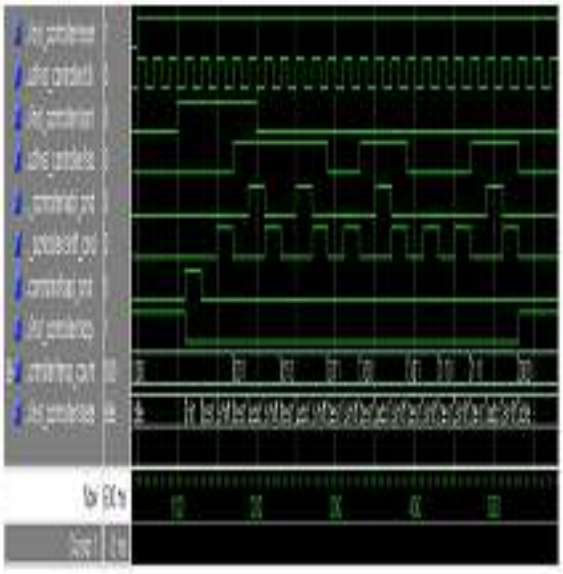

Fig 4 Multiplicand

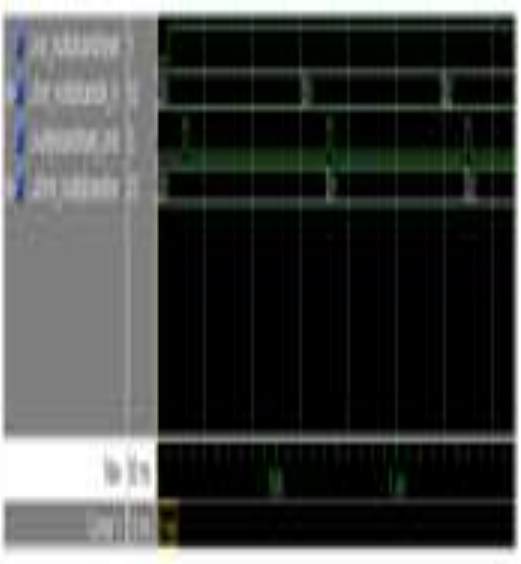

Fig 5. Control

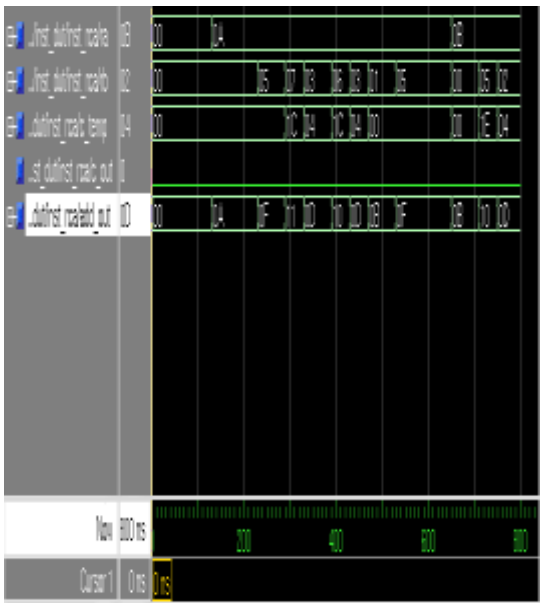

Fig 6 Multiplier Result

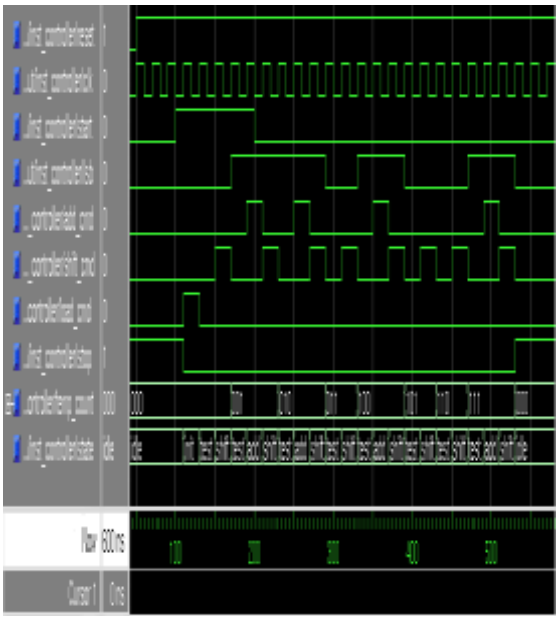

Fig 7 Ripple Carry Adder

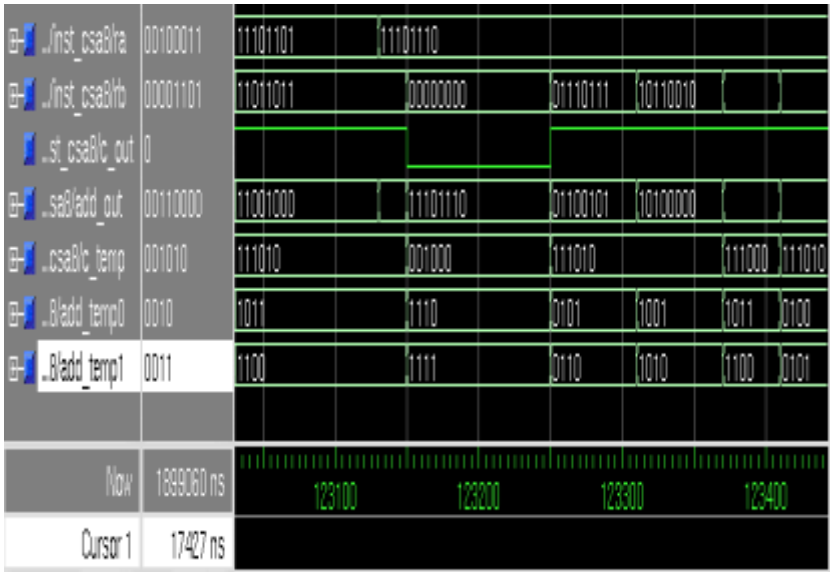

Fig 8 Carry Select Adder

IV. CONCLUSION

The goal of the project, to design multiplier using the DM^2 adder, was achieved. The multiplier was designed, coded in VHDL and simulated using the appropriate caddence tools. As an added value to the project, several designs were implemented in order to compare speed and area. Designs were also synthesized using various targets. The place & route for the modules are going on. As mentioned, the energy dissipation is reduced and performance is increased.

V. NOMENCLATURE

DM^2 – Dual Mode Square Adder.

VHDL – V (VHSIC- Very High Speed Integrated Circuit) Hardware Description Language

LSB – Least Significant Bit

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