DESIGN OF LOW POWER CMOS LOW NOISE AMPLIFIER USING CURRENT REUSE METHOD-A REVIEW

Hardik Sathwara[1], Kehul Shah[2]

[1]PG Scholar, [2]Associate Professor, Department of E&C, SPCE, Visnagar, Gujarat, (India)

ABSTRACT

LNA is one of the most important building blocks in the front end of the wireless communication systems. Amplification of weak signal and attenuation in noise level is a key role of LNA. In recent years valuable research is done on CMOS LNA design in on improvement of low power consumption, low noise figure, high gain, smaller space and low supply voltage. This paper illustrates a review work regarding the low power LNA design. The paper describes some fundamentals of LNA, designing method for low power LNA and design steps. This paper will be beneficial for primary stage of CMOS LNA design with low power consumption.

Keywords: Current Reuse Method, Lna, Low Power Consumption

I. INTRODUCTION

Wireless communication system is an integral part of day today communication. For effective wireless communication, faithful trans-reception of the signal is required. It can be achieved by careful design of the receiver circuit. Radio frequency design has been one of the major research areas in these days. Evolution of several Wireless Communication standards has demanded availability of different analog blocks for use in transceivers with different parameters, imposed by the nature of application. Particularly, lot of research has been carried out in CMOS technology, due to its high speed and low cost nature.

Any communication system must require transmitter and receiver for exchange of data or information. The design of wireless receiver is big task as receiver faces various external as well as internal design issues. In wireless receiver low noise amplifier (LNA) is a critical building block that amplifies the received signal and contributes most of the noise figure of whole receiver. LNA is an integral component of RF receiver and mostly required to operate at wideband frequency range. LNA performs various functions i.e. to amplify the signal, reduction of noise, reduce Noise Figure (NF), increase gain, improve stability and eliminate channel interference [1]. But the most important function is to amplify signal with low noise amplification [2,3].

The communication system that consists of transmitter and receiver will face not only attenuation but also the interference at the receiver end [4,5]. The received signal is so weak to use for demodulator so that it is necessary to amplify it with minimum noise amplification. So, LNA is most essential active block in receiver front end chain. LNA is situated between RF filter and mixer as shown in Fig. 1 [1].
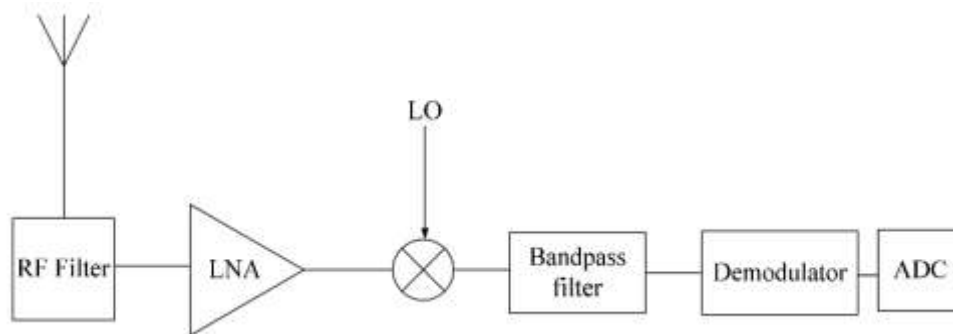
Fig.1: Block diagram of simple receiver front end

The primary challenge in LNA design is to achieve maximum input matching and low noise at any given power. Therefore, many kinds of LNA topologies have been proposed to satisfy the requirements for good performance at low power dissipation [5,6]. From the survey of recent years' works on LNAs, it is concluded that a low power LNA is required while providing high gain, low NF and better linearity. So, a special attention has to be paid to develop low power techniques for CMOS RF circuit.

During literature survey, it is found that Current Reuse Technique is one of the best methods used to design low power high gain LNA. In this paper, chapter II includes brief description of LNA using current reuse method. Design methodology and design steps are included in chapter III. Chapter IV describes design flow of LNA which is followed by conclusion and references.

II. CURRENT REUSE METHOD

The current-reuse topology may provide the best combination of high power gain, low noise figure, and low power consumption, making it a feasible option for use in UWB LNA designs [5]. In an amplifier employing current-reuse techniques, the input RF signal is amplified by two cascaded common-source amplifier stages to provide high gain. At the same time, this topology also supports low noise figures. The input matching circuitry is aided by a high-pass filter to suppress noise [8]. The basic issue with using CMOS transistor for LNA is its inherently low transconductance and hence low gain. However, if current reuse method is used, transconductance would be increased. The key point is that given the same bias current the effective transconductance is $g_{m1} * g_{m2}$, while it is simply g_m in other cases. That's why due to single source it dissipates low power [5].

The current reused model can be considered as a two stage cascade amplifier, in which the first stage is the CS amplifier and the second stage is the cascode amplifier with an additional buffer stage at output end [8].

The current-reuse technique is well known for its use in LNAs, for its capability of achieving high performance with power consumption that is less than conventional two-stage common-source amplifiers Fig. 2(a). In such a design approach, transistors M_1 and M_2 are connected as a cascade structure by means of coupling capacitor C_1; load inductor L_{load} and load resistor R_{load} are the loads for transistors M_1 and M_2; and currents I_{D1} and I_{D2} are the drain currents for transistors M_1 and M_2. [5,8,9]
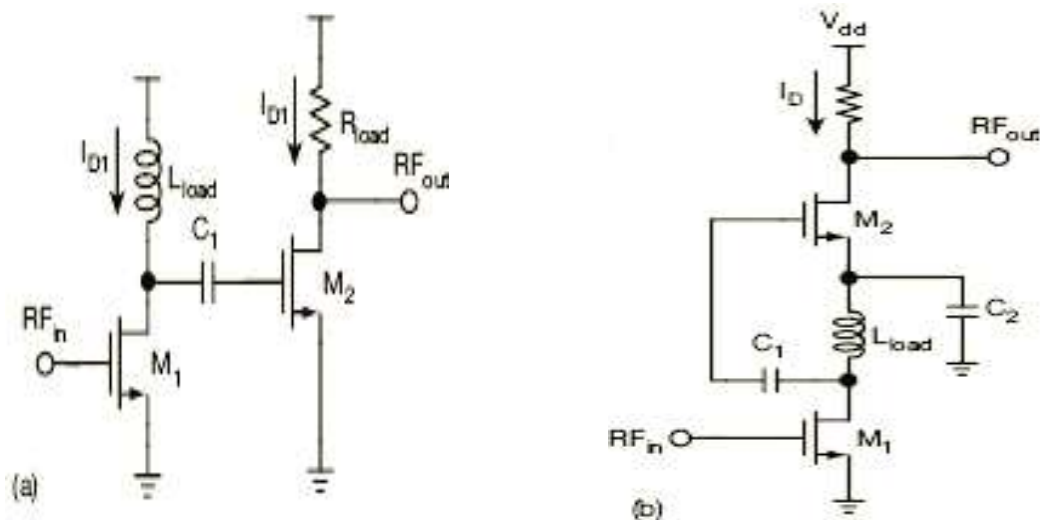
Fig. 2(a): Conventional Two stage CS amplifier, Fig. 2(b): Conventional Current Reuse method

Fig. 2(b) shows the schematic diagram for the two-stage current-reuse common-source amplifier, with C_2 used as a bypass capacitor. It can be seen that currents I_{D1} and I_{D2} can be reused as current I_D; there is just one current path between drain voltage V_{DD} and ground. In the experimental current-reuse LNA, the amplifier topology has been transformed from a two-stage common source structure without changing the essential amplifier type, resulting in high gain without adding power consumption.

Current Reuse topology can be used with any circuit configuration like cascode topology, common source or common gate, and feedback topologies or even with multi stage cascaded structures to reduce the DC power consumption. A major drawback of current reuse method is its high input & output impedances thus, it require external impedance matching [5,10].

III. DESIGN METHODOLOGY

The design methodology for LNA with current reused method is as below [11]:

Step- 1: In Fig. 3 given below, C_{gs} is the parasitic capacitance and L_2 is source degenerated inductor. All other parasitic effects are ignored. So, input impedance is derived by using equation (1):
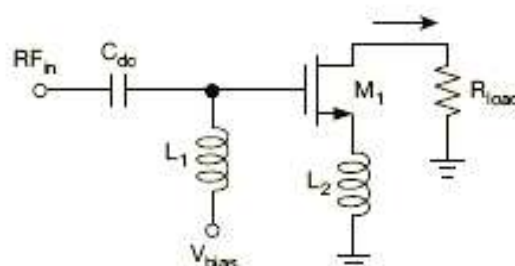

Fig. 3: Input impedance network for current reuse method

$$Z_{in} = \frac{1}{sC_{dc1}} + sL_1 \;||\; (\frac{1}{sC_{gs}} + sL_2 + \frac{g_m}{C_{gs}}) \;||\; R_{Load} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (1)$$

Step- 2: The experimental current reuse LNA employs an internal CS configuration with two stages. The voltage gain of CS amplifier can be calculated using equation (2):

$$A_v = g_m (r_0 \;||\; R_L) \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (2)$$

Where:

r_0 = the output resistance of transistor M_1

R_L = the load resistance.

Step- 3: From Figure 4.1(b), we can obtain equivalent gain circuit as shown in Fig. 4. This circuit is divided into two stages. The Voltage gain of first stage is found by using equation (3):
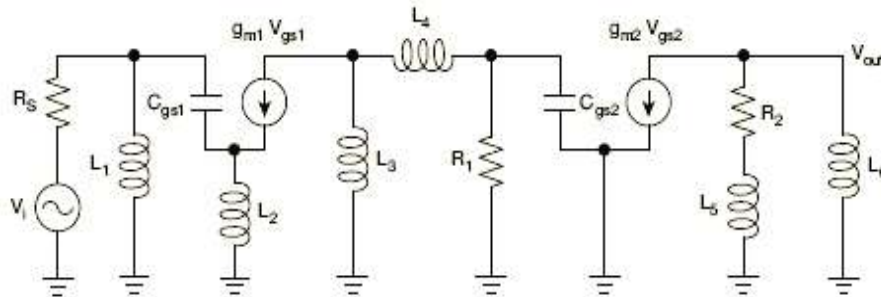

Fig. 4: Equivalent gain circuit of Fig. 2(b)

$$A_{v1} = - g_{m1} \cdot \frac{sL_3 \, || \, (sL_4 + R_1)}{1 + sL_2 (g_m + sC_{gs})}$$ …………………………………………….. (3)

Step- 4: The Voltage gain of second stage is calculated by means of equation (4):

$$A_{v2} = - g_{m2} \cdot \{ (R_2 + sL_5) \, || \, sL_6 \}$$ …………………………………………. (4)

Step- 5: The Voltage gain of overall circuit is shown in equation (5):

$$A_v = A_{v1} \times A_{v2}$$

$$A_v = g_{m1} \cdot g_{m2} \cdot \frac{sL_3 \, || \, (sL_4 + R_1)\{R_2 + sL_5 \, || \, sL_6\}}{1 + sL_2 (g_m + sC_{gs})}$$ ……………………………. (5)

Step- 6: One of the key performance parameters in the design of any LNA is noise figure which, in general, sets the noise figure for the first stage of a receiver. Noise figure is additive in an LNA, depending on the number of stages, with the noise of the first stage having the greatest impact on the overall noise figure of a multistage amplifier. The total noise figure of a multistage LNA circuit configuration, F_{total}, can be found from equation (6):

$$F_{Total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 \cdot G_2} + \dots$$ …………………………………….. (6)

Where:

F_1 = the noise figure of the amplifier's first stage and

G_1 = its gain

IV. DESIGN FLOW

The design procedure is depicted in Fig. 5. The design process starts with the calculation of transistor size. Then after, we will calculate the values of all components like resistors, capacitors and inductors. After calculation, optimization is applied; if we don't get desired results then whole process is repeated using iteration.
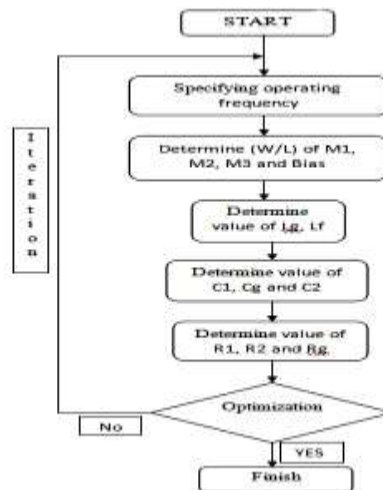
Fig. 5: Design flow diagram

V. CONCLUSION

This paper presents the theory of low power CMOS LNA design. During the survey, it is found that current reuse method is one of the best methods used to design low power LNA. Current reuse method is described here with simple design methodology. As per the recent scenario low power consumption is big task to every electronics device. So, this paper will be guide in the direction of low power design of LNA.

VI. ACKNOWLEDGEMENT

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