PERFORMANCE ANALYSIS OF INVERTER GATE USING FINFET AND PLANAR BULK MOSFET TECHNOLOGIES

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ABSTRACT

Due to scaling of metal-oxide-semiconductor field-effect ransistors (MOSFETs) with each new generation of CMOS technology has provided us with improved circuit performance and cost per function over several decades. But, continued transistor scaling will not be straightforward in the sub-32 nm regime because of fundamental material and process technology limits. The main challenges in this regime are twofold: (a) minimization of leakage current (subthreshold and gate leakage), and (b) reduction in the device-to-device variability to increase yield. Fin field effect transistors (FinFETs) have been proposed as a promising alternative for addressing the challenges posed by continued scaling. Fabrication of FinFETs is compatible with that of conventional CMOS, thus making possible very rapid deployment to manufacturing. The primary objective of this paper is comparative analysis of the design and performance of logic gates based on CMOS and FinFET technologies In this work, the inverter gate is modeled in HSPICE software on 32nm technology node using CMOS structures and FinFET structure are analyzed and their performances like power consumption is compared.

Keywords: MOSFET, FinFET, HSPICE, Power Consumption

I. INTRODUCTION

Currently, bulk CMOS technology is facing great challenges due to increased leakage and process variations with shrinking device dimensions. Even with advanced fabrication techniques, the scalability of bulk CMOS is limited due to increased leakage and short-channel effects (SCEs). This has motivated researchers to look for non-classical silicon devices to extend CMOS scaling beyond 22-nm node. A large number of recent works suggest that double gate (DG) devices are the best alternatives. Among the various types of DG devices, quasi-planar FinFET is easier to manufacture compared to planar double gate devices. FinFETs employ very thin undoped body to suppress subsurface leakage paths and, hence, reduced SCEs. An undoped or lightly doped body eliminates threshold voltage (*Vt*) variations due to random dopant fluctuations and enhances carrier transport resulting in higher on current.As the dimensions of transistors are shrunk, the close proximity between the source and the drain reduces the ability of the gate electrode to control the potential distribution and the flow of current in the channel region, and undesirable effects, called the “short-channel effects” start plaguing MOSFETs. For all practical purposes, it seems impossible to scale the dimensions of classical “bulk” MOSFETs below 20nm. If that limitation cannot be overcome, Moore’s law would reach an end around year 2012.

There exists a simple tool, called the Voltage-Doping Transformation model (VDT),that can be used to translate the effects of shrinking device parameters such as gate length or drain voltage into electrical parameters. In the particular case of the Short-Channel Effect (SCE) and the Drain-Induced Barrier Lowering (DIBL), the following expressions can be derived from the VDT model:

$$SCE = 0.64\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\left[1+\frac{x_j^2}{L_{el}^2}\right]\frac{t_{ox}}{L_{el}}\frac{t_{dep}}{L_{el}}V_{bi} = 0.64\frac{\varepsilon_{Si}}{\varepsilon_{ox}}EI\,V_{bi} \quad (1.1)$$

and

$$DIBL = 0.80\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\left[1+\frac{x_j^2}{L_{el}^2}\right]\frac{t_{ox}}{L_{el}}\frac{t_{dep}}{L_{el}}V_{DS} = 0.80\frac{\varepsilon_{Si}}{\varepsilon_{ox}}EI\,V_{DS} \quad (1.2)$$

where Lel is the electrical (effective) channel length, Vbi is the source or drain built-in potential, tox is the gate oxide thickness, xj is the source and drain junction depth and tdep is the penetration depth of the gate field in the channel region, which is equal to the depth of the depletion region underneath the gate in a bulk MOSFET. The parameter EI is called the “Electrostatic Integrity” factor. It depends on the device geometry and is a measure of the way the electric field lined from the drain influence the channel region, thereby causing SCE and DIBL effects. Based on the above expressions, the threshold voltage of a MOSFET with a given channel length Lel can be calculated using the following relationship:

$$V_{TH} = V_{TH\infty} - SCE - DIBL \quad (1.3)$$

where VTH∞ is the threshold voltage of a long-channel device. The decrease of threshold voltage with decreased gate length is a well-known short-channel effect called the “threshold voltage roll-off”. As can be seen from these expressions, short-channel effects can be minimized by reducing the junction depth and the gate oxide thickness. They can also be minimized by reducing the depletion depth through an increase in doping concentration. However, gate oxides cannot be scaled beyond a certain threshold because of the increasing tunneling current associated with smaller gate-oxide thicknesses. Another technique, which is used to mitigate short-channel effects, is to reduce the depletion width below the channel to the substrate.A reduced depletion width corresponds to shortened depletion regions and, hence, reduced parasitic capacitances. This results in improved subthreshold slope in the leakage regime. However, a reduction in the depletion width corresponds to degraded gate influence on the channel, which leads to a slower turn on/off of the channel region.Short-channel effects arise when control of the channel region by the gate is affected by electric field lines from source and drain.

These field lines are illustrated graphically in Fig1. In a bulk device (Fig. 1 A), the electric field lines propagate through the depletion regions associated with the junctions. Their influence on the channel can be reduced by increasing the doping concentration in the channel region. In very small devices, unfortunately, the doping concentration becomes too high (1019 cm^{-3}) for proper device operation.

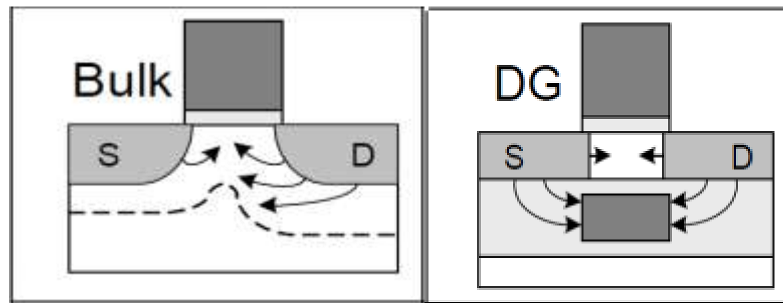

Fig1: Encroachment Of Electric Field Lines From Source And Drain On The Channel Region A: Bulk MOSFET; B: Double-Gate MOSFET.

The Voltage-Doping Transformation model can gave the Electrostatic Integrity factor of a bulk device can be written:

$$EI = \left[1 + \frac{x_j^2}{L_{el}^2}\right] \frac{t_{ox}}{L_{el}} \frac{t_{dep}}{L_{el}} \qquad (1.4)$$

In a double-gate device, both gates are connected together. The electric field lines from source and drain underneath the device terminate on the bottom gate electrode and cannot, therefore, reach the channel region (Fig. 1 B). Only the field lines that propagate through the silicon film itself can encroach on the channel region and degrade short-channel characteristics. This encroachment can be reduced by reducing the silicon film thickness.In double-gate device the effective junction depth and the effective gate field penetration for each gate is equal to tSi/2.

The Voltage-Doping Transformation model can gave the Electrostatic Integrity factor of a double-gate device, can be written as

$$EI = \frac{1}{2}\left[1 + \frac{t_{Si}^2/4}{L_{el}^2}\right] \frac{t_{ox}}{L_{el}} \frac{t_{Si}/2}{L_{el}} \qquad (1.5)$$

An important conclusion can be derived from the data presented in equation 1.5: bulk transistors run out of steam once they reach a gate length of 15-20 nm but smaller gate lengths can be only achieved by the double-gate structure.

In Section II and Section III, I gave the overview of the MOSFET and FinFET technologies. In Section IV advantages of FinFET over traditional MOSFET discussed. In section V and section VI presented FinFET circuits, parameters and result used by researchers. In section VI simulation results are presented. I conclude the paper in Section VII.

II. MOSFET TECHNOLOGY

Metal-Oxide Semiconductor Field-Effect Transistor or simply called MOSFET is another type of transistor besides Bipolar Junction Transistor (BJT). The first MOSFET is invented by Kahng and Atalla in 1960 which contribute to cost-effective for a large number of transistors on a single silicon chip compared to BJT. MOSFET is a four terminal device (drain, source, gate and bulk) where the amount of current flows between source and drain terminals is determined from the voltage applied to the gate terminal. At a certain level, this transistor also can be considered as a switch. When the gate voltage applied is greater than the threshold voltage, a conducting channel is developed between the drain and source, allowing for current to flow between the two terminals.

Otherwise, if the gate voltage applied is less than the threshold voltage, no conducting channel will be developed and the transistor is considered as an open circuit. Threshold voltage, Vth is the value of gate-to-source voltage when strong inversion occurs.

There are types of MOSFET devices that can be identified. The n-channel MOS or NMOS transistor consists of p-type substrate, n-type drain and n-type source.

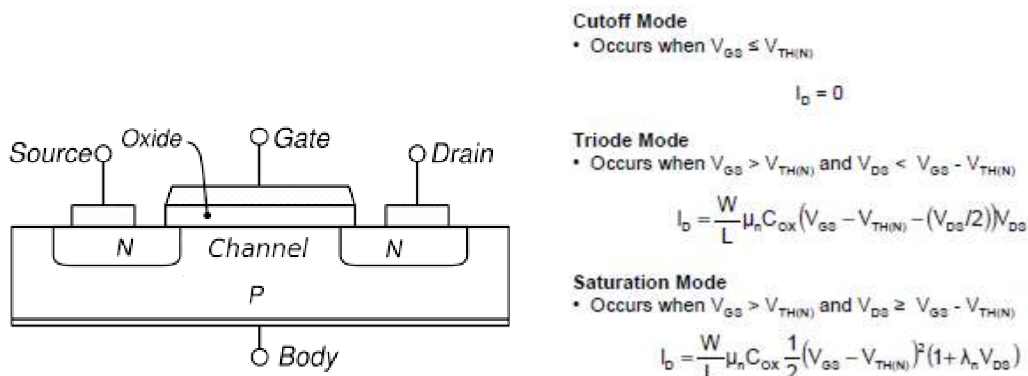

Fig2: N-Channel MOSFET

The other type of MOSFET is PMOS or p-channel MOS which consists of n-type substrate and p-type drain and p-type source.

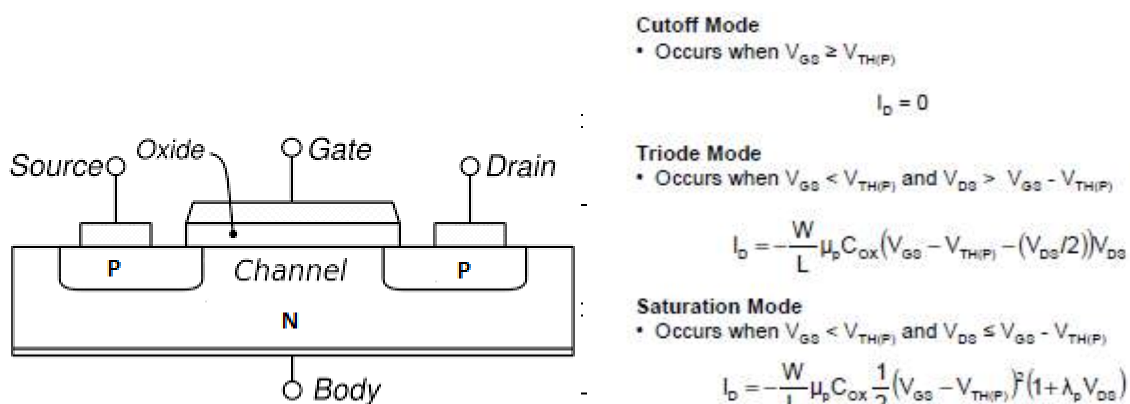

Fig3: P-Channel MOSFET

When both transistors are used in a circuit, the circuit is now called as Complementary MOS or CMOS circuits. Besides that, each type of transistor as mentioned previously also can be characterized into two categories which are enhancement mode and depletion mode. Enhancement mode transistor has no channel under the oxide layer that connects drain and source. The drain and source terminals will be connected only when a positive gate voltage is applied, which induces the electron inversion layer under oxide layer. The depletion mode transistor has channel that readily exists under oxide layer. The channel can be an electron inversion layer or an intentionally doped impurity. The existence of channel allow direct connection between drain and source terminals.

III. FINFET TECHNOLOGY

FinFET is a non-planar device having 'fin' like shaped where the gate is wrapped around and over the fin which acts as a transistor channel. It is also termed as quasiplanar device as the current flows parallel to wafer plane and the channel is perpendicular to wafer plane.

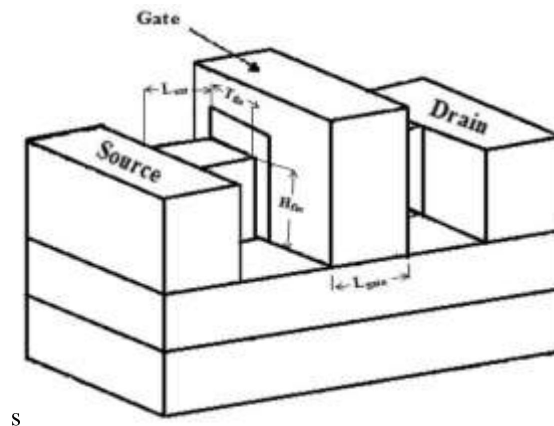

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Fig4: Structure of FinFET

Basically, FinFET was designed to be constructed on silicon-on-insulator (SOI) wafers. But the recent research has made it possible for FinFETs to work on bulk silicon wafers and improve the performance of certain parameters.

Effective channel length $Leff = Lgate + 2\times Lext$ (1)

Effective channel width $W = Tfin + 2\times Hfin$ (2)

Where Hfin and Tfin the fin height and thickness respectively, Lgate is length of the gate, Lext is extended source or drain region as explained in Fig 1. Fin widt (Tfin) plays a major role for controlling the short channel effect effectively. Therefore Tfin ~ Lgate/2 is followed.

In a FinFET structure, an ultra-thin Si fin forms a conducting channel wherein the electrons flow from source to drain. This conducting channel is wrapped by gate where the input voltages are supplied. Hence controlling the flow of electrons even in off state preventing the leakage of current. Sometimes there is an increase in the amount of charge carriers and the rate at which it flows, resulting in the breakdown of the conducting channel formed by single fin. This blocks the flow of electrons from source to drain which ceases the current flow.The number of fins is increased in multi-gate field-effect transistors (MuGFET) which are constructed parallel to each other improving short channel effect. As the number of fins increases, the amount of charge carriers flowing from higher potential to lower potential also increases. Therefore, the rate at which the carriers flow is faster increasing the switching speed. The main advantage of multiple fins is better gate control over the conducting channel. Due to this, there is a reduction in current leakage. This attains high onstate drive current. FinFETs have various logic design stylesdesigning of different FinFETs, inverter can be conFigd in one of the subsequent modes:

- **Shorted-gate (SG) mode**, in this mode both gate are shorted and we get improved drive strength and have better control over the channel length
- **Independent-gate (IG) mode**, in which independent signals drive the two device gates, this may reduce the number of transistors in the circuit.
- **Low-power (LP) mode**, in which we are applying a low voltage to n-type FinFET and high voltage to p-type FinFET. This varies the threshold voltage of the devices which reduces the leakage power dissipation at the cost of increased delay.
- **Hybrid IG/LP-mode** is a combination of LP and IG modes.

IV. ADVANTAGES OF FINFET OVER TRADITIONAL MOSFET

Table1: Advantages of FinFET over Traditional MOSFET

MOSFET	FinFET
The main obstacle is that thecontrol of current leakage is difficult.	The presence of multiple finshelps reduce leakage currents.
It is difficult to obtain higher on currents in bulk MOSFET.	It is easier to obtain higher oncurrents using multiple fins
Power Dissipation is more	Power Dissipation is less
It is a planar device as the current flows parallel to wafer and the channel is placed onwafer plane.	It is a quasi-planar device –asthe current flowsparallel to wafer and thechannel is perpendicular to wafer plane.
Only one gate is present to control the channel	Two gates are present to control the channel hence reducing short channel effect. This is available in Short Gate (SG) and Independent Gate (IG) mode.
Ioff -the drain current when Vgs=0, Vds=Vdd (Ideally 0)increases as it goes further away from the gate.	Due todouble gate, the gatecapacitance is doubled, hencelimiting Ioff (Ideally 0).(nand cmos vs finfet)

V. FINFETS CIRCUITS USED BY RESEARCHERS

[Feng Wang, et-al, 2006] proposed dependability (reliability and scalability) analysis of Nano-scale FinFET circuits. One of the biggest problems for nano-scale VLSI designers is guaranteeing dependability. Shrinking geometries, lower supply voltage, and higher frequencies, all have a negative impact on circuit dependability: the occurrences of soft errors increases due to these factors, and higher levels of device parameter variations change the design problem from deterministic to probabilistic. Consequently, reducing soft error rate and mitigating the impact of process variation are becoming increasingly critical. FinFET device was proposed as an elegant implementation of double-gate FET, which enables continuous technology scaling. Rainey *et al have* demonstrated the feasibility of FinFET logic implementation in 180nm, by showing inverter-chain operation for the first time. FinFET SRAM behavior was investigated by Joshi *et al* and it has been shown to exhibit higher performance and lower power compared against conventional planar PD-SOI. IBM was the first to convert an existing microprocessor designin a 100 nm FinFET technology and ensure its functionality.Guo et.al showed that FinFET-based SRAM design has a 30%improvement of noise margin over that of the bulk CMOS SRAM. Synopsys circuit simulator HSPICE tool is used for study FinFET behavior. The experiments compare FinFET circuits against bulk CMOS circuits in both 32nm and 45nm technologies. FinFET based designs provide the average of 83% and 43% reduction of the delay variation for logic gates and the memory cells over the designs in the Bulk CMOS. The results showing that FinFET circuits have better dependability and scalability, which is indicated by better soft error immunity and less impact of process variation on the performance. It is concluded that FinFET-based circuit designis more robust than the bulk CMOS based circuit design [13].

[Sherif A. Tawfik, et-al, 2008] evaluated group of new memory circuit techniques with the emerging FinFET technology. Presented and characterized independent-gate FinFET SRAM cells, multi-threshold voltage (multi-Vt) and the low threshold- voltage tied-gate FinFET SRAM cells ells and also compared for data stability, leakage power consumption, and cell area in a 32nm FinFET technology. The read stability is enhanced by up to 92% with the minimum sized dynamic independent-gate-bias FinFET SRAM cells as compared to the minimum sized low threshold- voltage tied gate FinFET SRAM cells in a 32nm FinFET technology. The idle mode leakage power and the cell area are reduced by up to 65X and 25.5%, respectively, with the work-function engineered multi-Vt FinFET SRAM cells as compared to a standard low threshold- voltage (low-Vt) tied-gate FinFET SRAM cell sized for comparable read stability [36].

[Zhiyu Liu, et-al, 2008] evaluated statistical data stability and leakage power of finfet SRAM cells with dynamic threshold voltage tuning under process parameter fluctuations. As the channel length of a conventional single gate- MOSFET is reduced to the nanometer scale, the drain potential begins to strongly influence the channel potential, thereby causing significant subthreshold leakage current. The multi-gate FinFETs offer significant advantages for suppressing the subthreshold and the gate dielectric leakage currents in the deeply scaled nanometer technologies. Proposed a new SRAM cell based on an independent-gate FinFET technology for simultaneously enhancing the read data stability and the memory integration density while reducing the active and standby modes power consumption. IG-FinFET SRAM technique is evaluated with the statistical data produced under process parameter variations in a 32nm FinFET technology. The average leakage power consumption of the IG-FinFET SRAM circuits is reduced by 51.2% and 53.3% at 70°C and 27°C, respectively, as compared to the tied-gate FinFET SRAM circuit with comparable data stability. Furthermore, the average read SNM of the IG-FinFET SRAM cell is enhanced by up to 82% as compared to the standard tied-gate FinFET SRAM cells under process parameter variations. Thus, proposed technique is best suited for the given problem [49].

[Ajay N. Bhoj, et-al, 2009] author addressed a gated-diode DRAM design in FinFET technology using mixed-mode 2Ddevice simulations. Increased scaling has placed considerable stress on SRAM technology due to the effects of process variations on performance, stability and standby leakage power consumption In order to circumvent the SRAM scaling/variability problem, researchers have considered replacing bulk SRAM with 2T/3T1D bulk DRAM or switching to a multi-gate implementation. Author addressed the above design problem in FinFET technology, in the light of process variations, by performing mixed-mode 2D device level simulations in a double gate design environment, called FinE that is developed. As concluded Gated-diode FinFET DRAM is an attractive choice for low-power, high-activity cache memories of the future [4].

[Dhruva Ghai, et-al, 2013] author investigated mixed-signal design for double-gate (DG) FinFET technology using a current-starved voltage controlled oscillator (VCO) as a case study. The use of conventional planar single gate MOSFETs is becoming extremely difficult due to enhanced Short-Channel Effects (SCEs). In addition to SCEs, planar MOSFETs suffer from random dopant fluctuations (RDF) in the channel area, which is believed to be the main source of threshold voltage mismatch among the devices fabricated on the same wafer. Author presented FinFETS technology in which process variation due to Random dopant fluctuations (RDF) are reduced due to undoped or lightly doped body and reduced carrier mobility degradation. From the process variation analysis, we observe that the FinFET VCO shows 4.66% variability due to *VTh* fluctuations, as compared to 18.98% variability in the CMOS VCO, making FinFETs more process variation tolerant. The major advantages of FinFET include the following: (1) nearly ideal subthreshold slope. (2) Small intrinsic gate

capacitance. (3) Smaller junction capacitances. (4) Better immunity to SCEs. (5) Higher (*ION/IOFF)* ratio. (6)Design flexibility at circuit level with shorted gate (SG) and independent gate (IG) options. As part of future research, thermal effects will be examined, as FinFETs suffer from self heating[12].

[Dhruva Ghai, et –al, 2013] presents an effort in the direction of exploring the FinFET technology for analog circuit design and summarized as follows: (1)A comparative analysis among the configurations of the FinFET device is presented for analog circuit design, (2) Output resistance, transconductance, Open-circuit gain, transition frequency is analyzed in both strong inversion and subthreshold regions, (3)Statistical process variation analysis is presented for the above FinFET parameters in both strong inversion and subthreshold regions of DG FinFET operation and (4) Design guidelines are formed for the analog circuit designer working with FinFET configurations. Nanoscale bulk CMOS technology suffers from various short channel effects (SCEs), threshold voltage fluctuations, and process variations. FinFET technology is used to get higher immunity to SCEs and process variation. Analyzing DG FinFET parameters in strong inversion region in LP mode the value of gm is 366.5 µS, r0 is 70.88 kΩ, open circuit gain is 25.98 and ft is 149.9 GHz. Analyzing DG FinFET parameters in subthreshold region in LP mode the value of gm is 12.4 μS, r0 is 3.7466 MΩ, open circuit gain is 46.45 and ft is 11.34 GHz. The future work will involve designing state-of-the-art analog circuits like bandgap references, op-amps and comparators using a blend of the various configurations studied in this paper [15].

[Manorama, et-al, 2013] designed and developed a FinFET Based Inverter Using MTCMOS and SVL Leakage Reduction Technique. Scaling of the Standard single-gate bulk MOSFETs faces great challenges in the nanometer regime due to the severe short-channel effects that cause an exponential increase in the leakage current and enhanced sensitivity to process variations. Double-gate FinFET has better SCEs Performance compared to the conventional CMOS and stimulates technology scaling. Author described different mode of FinFET technology and performed the comparative analysis of stand-by leakage (when the circuit is idle), delay and the total power of the logic circuit. Simulations are done on Cadence Virtuoso tool at 45nm. MTCMOS and SVL effective circuit-level techniques are applied to design that provides a high performance and low power design by utilizing both low and high-threshold voltage transistor. Simulation result shows the FinFETs based inverter using SVL technique has 50-60% low leakage power than the normal FinFETS based inverter and 25-30% lower than the FinFETs based inverter using MTCMOS technique. FinFETs based inverter using MTCMOS technique consume 65-70% less power than the normal based inverter and 35-40% than the FinFETs based inverter using SVL technique respectively. For reducing the leakage power and delay SVL technique is better than the MTCMOS technique but power consumption in the SVL technique is more than the MTCMOS technique. It is conclude that this solution approach is best suited for the given problem [28].

VI. FINFET CIRCUITS, PARAMETERS AND RESULTS USED BY RESEARCHERS

Table2: FinFET Circuits, Parameters and Results used by Researchers

Reference	Circuit model used and Software Used	Result	Variable/Parameters used
13	SRAM& HSPICE	average of 83% and 43% reduction of the delay	• Supply Voltage (Vdd) = 0.9V • Physical Gate Length (L) = 32nm • Physical Oxide Thickness(Tox) =1.4nm

			• Fin - Height (H) = 65 nm • Body thickness (Tsi) =8.6nm
12	VCO & Cadence Virtuoso tool at 45nm	FinFET VCO shows 4.66% variability due to *VTh* fluctuations, as compared to 18.98% variability in the CMOS VCO	• Supply Voltage (Vdd) =0.9V • Threshold voltage (*VThn*)= 0.31V, VThp= -0.25V • Physical Oxide Thickness(Tox) = 1.5 nm • Fin - Height (H) =50nm • Fin thickness (tsi)= 8.4 nm • Channel doping $Nch(cm^{-3}) = 2 \times 10^{16}$
28	Inverter & Cadence Virtuoso tool at 45nm	FinFETs based inverter consume 65-70% less power than the normal based inverter	• Supply Voltage (Vdd) = 0.9V • Physical Gate Length (L) = 45nm • Physical Oxide Thickness(Tox) = 1.5 nm • Fin - Height (H) =50nm • Body thickness (Tsi) =8.6nm
4	DRAM & Sentaurus TCAD and the Spice3-UFD model, MATLAB	FinFET DRAM cell shows three orders of magnitude higher retention time at a higher read frequency.	• Supply Voltage (Vdd) = 1V • Physical Oxide Thickness(Tox) =1.2V • Fin - Height (H) =75nm • Body thickness (Tsi) = 15nm
49	SRAM & Cadence Spetra	average leakage power Spetra consumption of the IGFinFET SRAM circuits is reduced by 51.2% and 53.3% at 70°C and 27°C	• Physical Gate Length (L) =32nm • Effective channel length (Leff) =25.6nm • Physical Oxide Thickness(Tox) =1.6nm • Fin - Height (H) =32nm • Fin thickness (tsi) =8nm • Channel doping $Nch(cm^{-3}) = 2 \times 10^{15}$

VII. SIMULATION AND RESULT

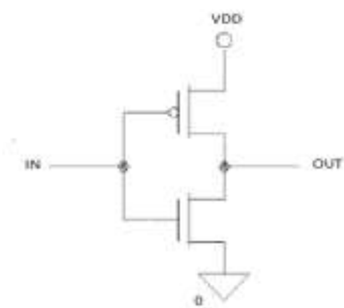
In this section, we present simulation results of 32nm FinFET based inverter and 32nm MOSFET based inverter and also average power calculation of the inverter gates of different mode using HSPICE. This below Table 2 shows the list of FinFET and MOSFET parameters which was used in the HSPICE simulation of inverter. These parameters were extracted from ITRS and IEEE Papers.

Table3: Parameters used in Experimentation

S.No.	Mosfet	Value	Finfet	Value
1	Technology node	32nm	Channel Length (L_g)	32nm
2	Supply Voltage(Vdd)	0.9V	Supply Voltage(Vdd)	0.9V
3	Vin(Input to inverter)	PULSE (0 0.9 3n .5n .5n 14n 20n)	Vin(Input to inverter)	PULSE (0 0.9 3n .5n .5n 14n 20n)
4	Capacitance	1f	Vhigh	1.2V
5	W&L (NMOS)	L=32nm W= 64nm	vlow	-0.1V
6	W&L (PMOS)	L=32nm W= 192nm	Capacitance	1f
7	Thickness of fin and channel (tsi)	8.6nm	Thickness of fin and channel (tsi)	8nm
8	Thickness of oxide(tox)	1.4nm	Thickness of oxide(tox)	NMOS =1.05nm PMOS =1.1nm
9	Channel dopping (Nch) (cm-3)	$4x10^{-18}$	Height of fin(Hfin)	16nm
10			Channel dopping (Nch) (cm-3)	$4 x10^{-16}$

7.1 MOSFET Based Inverter

The circuit diagram and input/output characteristics of MOSFET based inverter obtained is shown in Fig5 and Fig6 respectively. The supply voltages considered for the experimentation are 0.9V for 32nm technology. The input is taken in the form of a pulse.



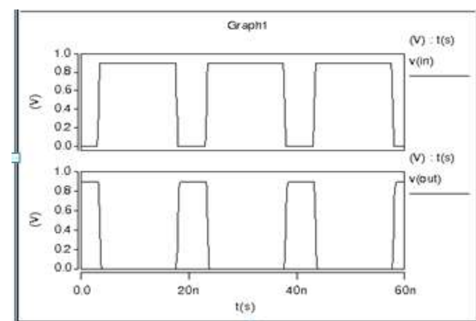
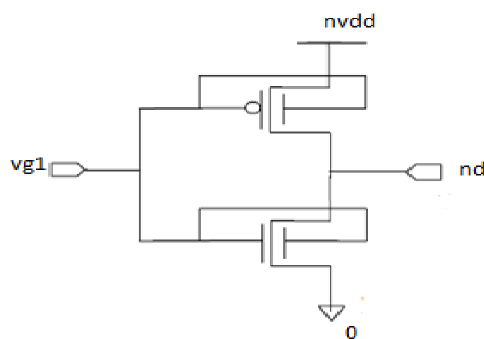


Fig5: Inverter Circuit using MOSFET **Fig6: Transient Analysis of MOSFET Based TechnologyInverter**

7.2 FinFET Based Inverter

The circuit diagram of inverter under FinFET technology Short-Gate (SG) mode, Low- Power (LP) mode, Independent-gate (IG) mode and Hybrid mode (IG/LP) according to FinFET technology is shown in Fig7, Fig8, Fig9 and Fig10 respectively. Simulate them in 32-nm technology node using H-SPICE software. Apply the inputs to the inverter circuit, propagate them through the inverter circuit and input/output characteristics FinFET based inverters obtained is shown in Fig11.



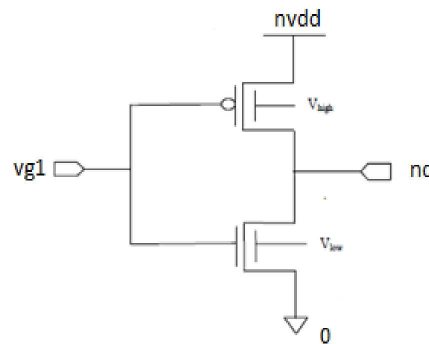
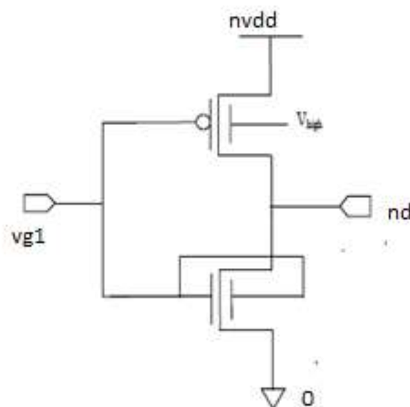


Fig7: Short-Gate (SG) Mode of Inverter Circuit using FinFET Technology

Fig8: Low-Power (LP) Mode of Inverter Circuit using FinFET Technology



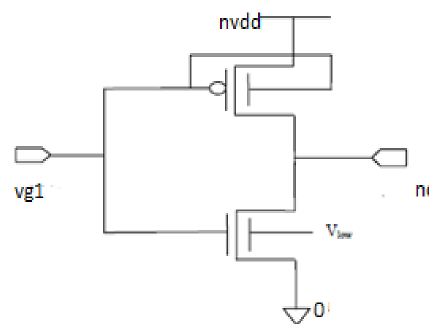


Fig9: Independent-Gate (IG) Mode of Inverter Circuit using FinFET Technology

Fig10: IG/LP Mode of Inverter Circuit using FinFET Technology

Table4: Comparison of Average Power

S. No	Technology	Methodology	Average Power
1	32nm	Planar Bulk MOSFT	1.5813E-07 watt
2	32nm	FinFET(SG Mode)	2.4988E-06 watt
3	32nm	FinFET(LP Mode)	6.2432E-07 watt
4	32nm	FinFET(IG Mode)	1.5868E-06 watt
5	32nm	FinFET(IG/LP Mode)	1.3091E-06 watt

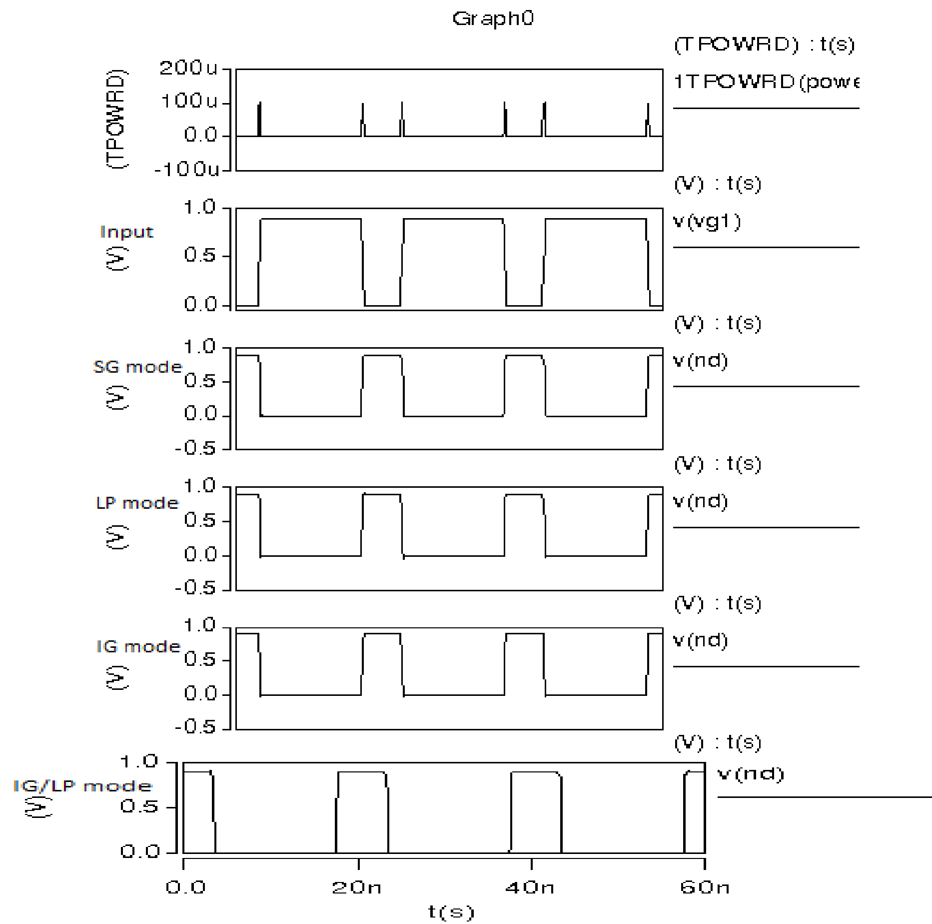


Fig11: Transient Analysis of SG, LP, IG mode and IG/LPmode FinFET Inverter

VIII. CONCLUSION

This Paper investigated the performance of the FinFET technology based Inverter and compared it with the existing silicon MOSFET technology using HSPICE. Simulation result shows that the average power consumption is much less compared to that of planar MOSFET based circuit in FinFET circuit (SG, LP, IG and hybrid mode).

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