EFFICIENT DIGITAL CIRCUITS BASED ON CNTFET

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ABSTRACT

This paper deals with basic logic circuits using the carbon nanotube field effect transistor (CNTFET). Due to various beneficial properties of carbon nanotubes, these circuits are more efficient than Metal Oxide Field Effect Transistor (MOSFETs). The parameters like power, delay and power delay product of CNTFET based circuits are compared with that of CMOS technologies. Both the simulations are performed in HSPICE software. The CNTFET based circuits provides more power reduction, delay reduction, and Power Delay Product (PDP) reduction when compared with CMOS technologies.

Keywords: Carbon nanotube (CNT), CNT field-effect transistor (CNTFET), Metal Oxide Semiconductor Field Effect Transistor (MOSFETs).

I INTRODUCTION

As per Moore's law, the number of transistors that are placed in an integrated circuit increases exponentially by almost doubling every two years. Continuously reducing the size of transistor i.e. scaling of MOSFET technology has been carried continuously in order to meet the density and sustain the IC predicted by Moore's law. Since in year 2006, the gate length of a MOSFET device has entered the deep submicron/nano regime at 65-nm feature size. Now-a-days, 45-nm technology is a reality used, and in the near future 32-nm has been predicted to be the feature size [1]. As the physical gate length is reduced to below 65-nm, several device-level effects, such as short channel effect, large parametric variations and exponential increase in leakage current, have substantially affected the I-V characteristics of traditional MOSFETs. This results in major concerns for scaling down the feature size of these devices. To meet the challenges of nano scale CMOS, and achieve similar performance like CMOS, CNTFET is explored. This CNTFET consists of utilizing new circuit techniques together with alternative technologies to replace conventional silicon and the current MOSFET-based technology [2].

1.1 Carbon Nanotubes (CNTs)

Carbon is the 4th most abundant element in the Universe by mass after (Hydrogen Helium and Oxygen) having atomic number of 6. It forms almost 10 million pure organic compounds with any other element. Carbon Nanotubes are long, thin cylinders of carbon, and were discovered in 1991 by Sumio Iijima of NEC Crop in Tokyo [2]. He proposed the new type of carbon structure which was needle like tubes of diameter varying from 4-30 nm. By survey of applications regarding to the transistors the channel of traditional MOSFET will replace by CNT. These are large that are unique for their size, shape, and remarkable physical properties. Carbon Nanotubes (CNTs) have attraction of researchers worldwide in recent years because of their small dimensions and unique

architecture properties. For passive or active elements in post-CMOS, Nano-electronics carbon Nanotubes is the best replacement device [3].

1.2 Carbon Nanotube Field Effect Transistor (CNTFET)

In the era of Nano scale, Carbon Nanotube Field Effect Transistor (CNTFET) is a promising device for future integrated circuits because of its tremendous properties like ballistic electron transport, high carrier mobility. In 1998, the first carbon nanotube field-effect transistors (CNTFETs) were reported. Which is one of the most promising alternatives to the MOSFET is the CNTFET. The most important and significant attribute of CNTFET is its spectacular ability in current carrying or current driving, and experiments have shown that CNTFET is the best for this purpose. CNTFET can operate five times faster than CMOS in the best case without any extra power overhead [3].

CNFETs are one of the molecular devices that avoid most fundamental silicon transistor restriction and have ballistic or near ballistic transport in their channel. Therefore a semiconductor carbon nanotube seems to be appropriate to be used as the channel of field effect transistors. Applied voltage to the gate can control the electrical conductance of the CNT by changing electron density in the channel. By using appropriate diameter suitable threshold voltage for CNFET can be achieved.

The threshold voltage of the CNFET is proportional to the inverse of the diameter of CNT and can be expressed as:

$$V_{th} = \frac{0.42}{D_{CNT}(nm)} \quad \text{(i)}$$

For a CNT with *(n, m)* as chirality and *a=0.249* as lattice (that is carbon to carbon atom distance) the diameter is:

$$D_{CNT} = \frac{a\sqrt{n^2+mn^2+m^2}}{\pi} \quad \text{(ii)}$$

As mentioned above, CNTs are used in CNFETs as channel and depending on the connections between source and drain with channel (CNTs) there are two main CNFETs. It works on the principle of direct tunneling through a Schottky barrier at the source–channel junction; therefore, these transistors are called Schottky Barrier CNFET (SB-CNFET). SB-CNFET shows ambipolar behavior and constrains usage of these transistors in conventional CMOS-like logic families. Schottky barrier restricts the trans-conductance in the ON state, and thus Ion/Ioff ratio becomes rather low. Second device is MOSFET-like CNFET which is doped in un-gated portions and has similar behaviour to CMOS transistors and it presents unipolar behaviour. The semiconductor junction will eliminate schottky barrier and therefore there is higher ON current unlike SB-CNFETs. Other advantages of MOSFET-like CNFETs are high on-off ratio and their scalability compared to their schottky barrier counterparts. In this paper we utilized MOSFET-like CNFETs for designing the logic gates [1].

II SPICE COMPATIBLE MODEL FOR CNTFET

CNTs are used in the channel region of the CNTFET. Different types of CNTFET have been demonstrated in the literature. There are mainly two types of CNTFET: Schottky barrier CNTFET (SB-CNTFET) and MOSFET-like CNTFET as shown Fig. 1. In SB-CNTFET the channel is made of intrinsic semiconducting CNT and direct

contacts of the metal with the semiconducting nanotubes are made for source and drain regions. The device works on the principle of direct tunneling through the Schottky barrier (SB) at the source-channel junction thus, the trans-conductance of the device is controlled by the gate voltage.

In MOSFET-like CNTFET doped CNTs are used for the source and drain regions and channel is made of intrinsic semiconducting CNT. A tunable CNTFET with electrical doping is also proposed. It works on the principle of barrier-height modulation by the application of gate potential.

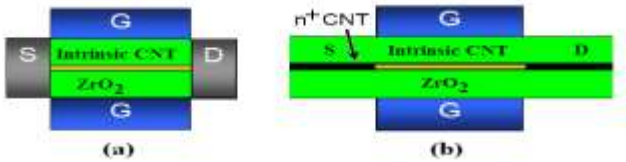

Fig. 1. Different types of CNTFETs: (a) Schottky barrier (SB) CNTFET (b) MOSFET-like CNTFET [4].

All the below circuits are simulated using Synopsys HSPICE 2008 simulator tool with SPICE model for CNTFET at 32nm technology. The CNTFET standard model has been designed for unipolar, MOSFET-like CNTFET device in which each transistor may have one or more CNTs [5]-[12]. The parameters of the CNTFET model and their values, with brief descriptions are shown in below Table I.

Table I: CNTFET Model Parameters

Parameter	Description	Value
Lch	Physical Channel Length	32 nm
Lgeff	Mean free Path in instrinsic CNT Channel	100 nm
Lss	Length of doped CNT source-side extension region	32 nm
Ldd	Length of doped CNT drain-side extension region	32 nm
Kgate=Kox	Electric constant of high K top gate electric material	16
Hox=Tox	thickness of high K top gate electric material	4 nm
Csub=Cb	Coupling Capacitance between channel region and substrate	40 pF/m
CNT pitch	Region of CNT tube placed	20 nm

III ANALYSIS OF LOGIC GATES

Different digital logic gates such as INVERTER, NAND, NOR, OR and combinational circuits have been designed using CNTFET. These logic gates/circuit are simulated by using HSPICE software. After simulation, the circuits have analyzed for their average power, delay and PDP (Power delay product). In Fig.2, the schematic design and simulation of combinational circuit is shown.

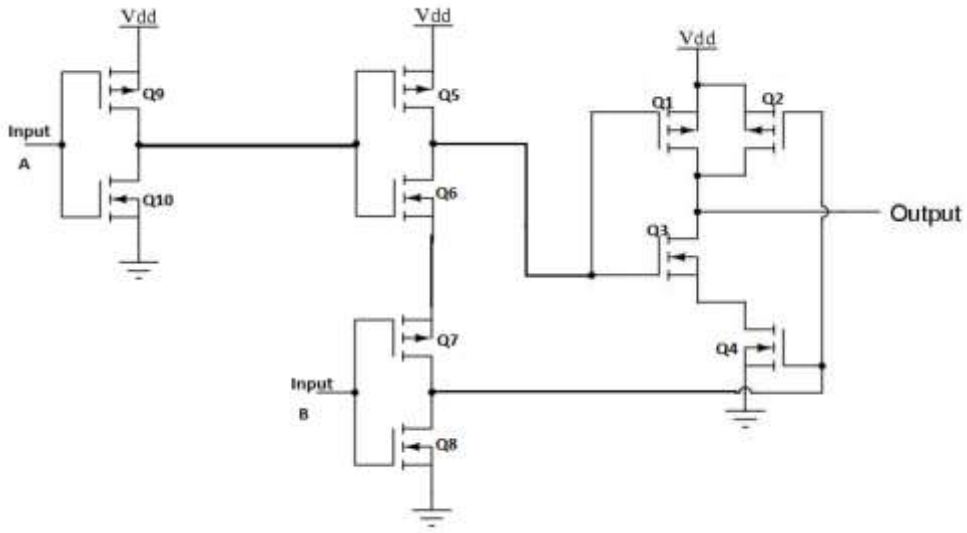

Fig. 2 Design of Combination Circuit Using OR and NOT Gate

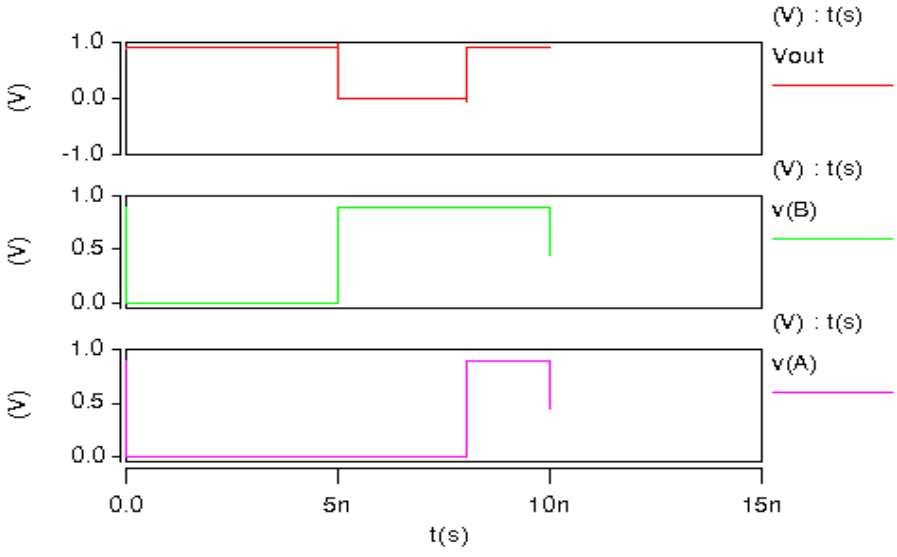

Fig. 3 Transient Response Using CNTFET

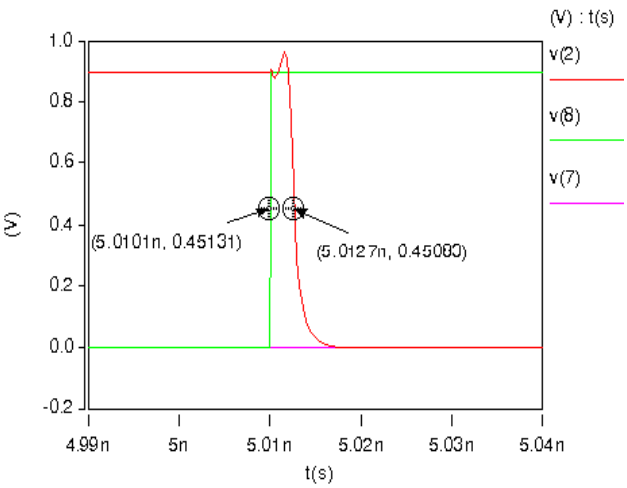

Fig.4 Transient Response Using CNTFET Showing Delay

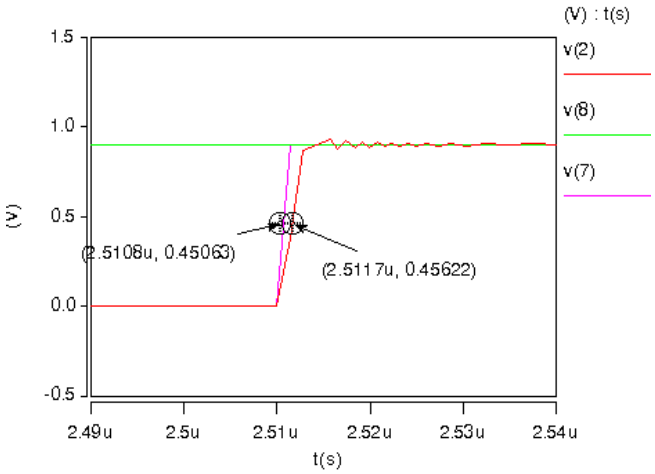

Fig. 5 Transient Response Using MOSFET Showing Delay

The design shown in Fig. 2 is obtained for Output=Y= Σm (0, 1, 3), i.e. $Y = \overline{A} + B$. In this way CNTFET inverter, NAND, NOR and OR gates have been simulated in HSPICE software for CNTFET model of 32nm technology. The performance parameter viz. power, delay and power delay product (PDP) have been calculated for these circuits and also for CMOS circuit design.

IV RESULTS

The circuit shown in Fig. 2 is verified using HSPICE software. The results obtained for power dissipation (P), Delay (D), and Power delay product (PDP) are tabulated in Table II and III. The result shows significant reduction in power dissipation, delay and hence power delay product.

TABLE II: Performance Analysis of CMOS logic gates at VDD=0.9V

CMOS			
Designs using logic gates	**P (J/Sec)**	**D (Sec)**	**PDP (J)**
INVERTER	9.9528E-07	4.4E-09	43.7923E-16
NAND	3.8244E-05	6.2E-09	23.7113E-14
NOR	8.0468E-07	2.1E-09	16.8982E-16
OR	1.8877E-6	6E-09	11.3262E-13
Combinational Circuit ($Y = \overline{A} + B$)	7.3781E-07	2.6E-09	19.1831E-14

TABLE III: Performance Analysis of CNTFET logic gates at VDD=0.9V

CNTFET			
Designs using logic gates	**P (J/Sec)**	**D (Sec)**	**PDP (J)**
INVERTER	4.0243E-09	4E-13	16.0972E-22
NAND	5.4986E-09	1.6E-12	8.7977E-21
NOR	8.9529E-09	10E-12	89.529E-22
OR	1.5163E-07	7E-12	10.6141E-19
Combinational Circuit ($Y = \overline{A} + B$)	1.1770E-08	3.1E-12	3.6487E-20

V CONCLUSION

This paper compares CNTFET based logic circuits with CMOS based logic circuits using HSPICE software. Simulations are carried at room temperature with voltage 0.9V and performances are studied by using parameters like power, delay, and PDP. The result shows that CNTFET based circuit design gives good performance like fast output response, less average power dissipation, and improved transient response than CMOS based circuits designs.

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