# VLSI IMPLEMENTATION OF HIGH SPEED ADC WITH COARSE AND FINE CONVERSION

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## ABSTRACT

*Analog-to-Digital converter (ADC) measures the maximum amplitude of an analog pulse and converts the value to a digital number. The digital output is a relative account of the analog amplitude at the ADC input. For consecutively incoming pulses, the digital outputs from the ADC are fed to a devoted memory, or a computer and sorted into a histogram. Multi-channel imaging detectors are extensively been used for both high-energy physics instruments and biomedical imaging devices .The multi-channel ADC can save both the die area power dissipation. To overcome the problem of long conversion time in the classic Wilkinson ADC, a new architecture using a counter and delay line interpolations are introduced. 5-bitGray counters are considered for the coarse conversion .The time interruption using a collection of five delay-locked loops (DLLs) and the multiphase sampling technique are proposed for the fine conversion. In multi-channel topology, the ramp generator and counter are shared by all channels.*

***Keywords: Analog-to-Digital converter (ADC), delay locked loops (DLLs), Gray counters.***

## I LITERATURE SURVEY

The most important features of single ramp ADC is valid for multi-channels, high resolution and low power dissipation applications. Imaging detectors are used to determine their energy, type of radiation and other parameters [1]. In wilkinson ADC the design of multi-channel, together with the A/D converter of completely integrated read-out circuit for spectrometry applications [2].This paper focus on multi-channel single ramp ADC for imaging detector applications. Since they contain low power dissipation, sampling rate improvement than the wilkinson ADC. Counter and ramp generator can be shared between the channels .So that the ADC part replicated in each channel can be reduced to a comparator and memory used to copy and memorize the counter state. The front-end readout chain is mostly collected of a charge sensitive amplifier (CSA), a pulse shaper, a peak-detect-and hold circuit, and an output buffer. Inside a number of suitcases a discriminator with a TDC might be engaged to provide the time stamps.

The weak signals (current or voltage) are composed by the CSA and twisted by the pulse shaper. There are some inherent restrictions of Wilkinson ADC [2]. These incorporate long conversion time and large power dissipation. Such as flash [5], pipeline[6] and successive - approximation - register (SAR) ADCs [7] are accessible for multi-channel applications. Although high speed can be achieved flash ADCs due to their large

power dissipation. In SAR and Pipelined ADCs is excellent choice for low power design. However, both SAR and pipelined ADC occupy large die size. In flash ADCs, three main sources of timing indecision are clock skew, data skew and random jitter of clock signal. Except the clock and data skew control if the ADC is determined by a low phase noise clock [4].

However , it is establish that the THA output ought to then be scattered to the comparators with a bandwidth of larger than the sampling frequency in order to conserve the flat regions of the track and hold waveform. To grouping of high sampling rate and high resolution, time interleaved enclose be confirmed in[10]. The rest of the paper contains Wilkinson and Successive - approximation ADC design. Section II give the concise summary of the Existing System. Section III analyses the power , sampling rate, resolution bits of the wilkinson, Successive - approximation and multi-channel ADC.

## II WILKINSON ADC AND SUCCESSIVE - APPROXIMATION ADC (SAR)

There are a variety of ADCs residential in earlier period to attain the multi-channel ADC architecture for spectroscope applications [9].

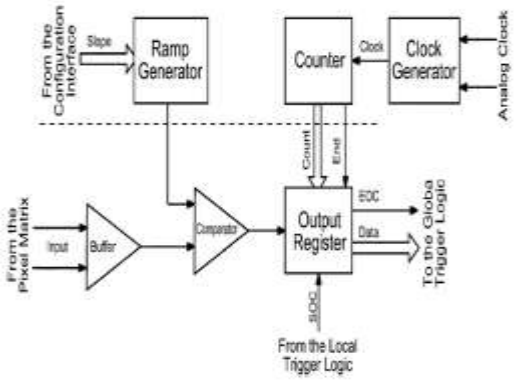


**Figure 1: Wilkinson ADC architecture**

Novel low-jitter delay-locked loops(DLLs) techniques are used to recover the resolution for multi-channel time-to-digital converters (TDCs) [15] devoid of allowing for the method of coarse and fine conversion.The wilkinson ADC architecture is shown in Fig.1 Meta stability effects are functional in [9] to minimizes the digital noise and decreases the power dissipation.

The ramp generator is realized by injecting a current in an integrator, implemented using an operational amplifier with capacitive feedback. The value of the current, and hence the slope of the ramp, is controlled with 7 bits. The front-end circuit includes also a digital part, which consists of a current mode amplitude discriminator; a voltage mode peak discriminator and a logic circuit for reset and pulse pile up rejection. The ramp generator, the counter and the clock generator are common to all of the A/D converters of the array, while here is an input buffer, an output register and a comparator associated with each row of the array.

The comparator compares the front-end circuit output signal, which is a constant voltage proportional to the incident photon energy, with the ramp produced by the ramp generator.

When the counter reaches full scale, the output register produces the end-of conversion (EOC) signal. It consumes low power for 3.3v power supply. The system allows us to process the signal provided by the detector down to the final A/D conversion, which is pretty uncommon for spectroscopic read-out channels, where the

A/D conversion is typically performed off-chip. Repeatability of drop orientation is critical to measuring a repeatable response.

## III SUCCESSIVE-APPROXIMATION ADC (SAR)

The general circuit diagram of successive-approximation ADC is shown in Figure 2 . During the rise of the analog input pulse, the switch S1 is closed and the voltage on capacitor C1 tracks the rise of the input signal. When the input signal reaches maximum amplitude, S1 is opened, leaving C1 holding the maximum voltage of the input signal

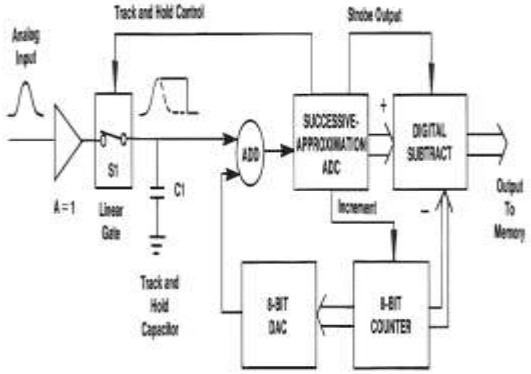


**Figure 2 : Circuit diagram of Successive-Approximation ADC**

A n-bit SAR converter utilizes only one comparator with basically clock cycles to complete a full conversion, which can clearly result in an area and power efficiency advantage over other architectures, such as flash topologies, showing an exponential relation with the number of bits.

The SAR algorithm is executed asynchronously by adjusting the comparator threshold at runtime to match the input signal. Since the comparator is fully dynamic, the architecture is power-scalable, showing power consumption basically proportional to its activity. Moreover, since the ADC has built-in thresholds, there is no need for external reference generation and buffering. This binary number Nc is the address of the memory location to which one count is added to build the histogram representing the pulse-height spectrum. If the ADC has n bits (2n channels), n test cycles are required to complete the analysis, and this is the same for all pulse amplitudes.

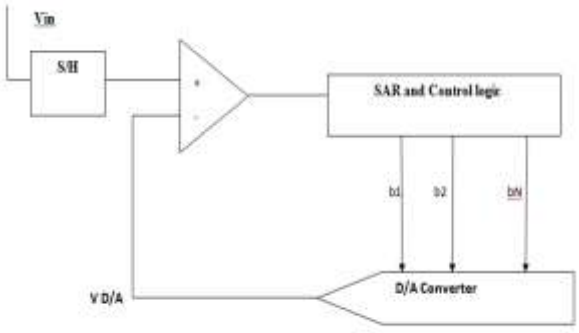


**Figure 3 : Typical SAR ADC architecture**

A typical SAR ADC architecture is shown in Figure 3. It consists of a S/H stage, a comparator, a digital controller and a digital-to-analog converter (DAC). In a SAR ADC, the DAC output voltage successively approximates the sampled input voltage. It occupy large die size ,and the design of SAR ADC is very complicated. The TC comparator was operated from a dedicated 1-V analog supply voltage, while controller and digital buffers could be operated from a supply as low as 0.7V, thus trading speed with 240µW power consumption. It is not applicable for multiple channel.

## IV MULTI-CHANNEL SINGLE RAMP ADC

The basic architecture of the proposed scheme is multi-channel single ramp ADC for generating the 12-bit resolution. Compared to wilkinson ADC the proposed multi-channel ADC architecture uses the coarse and fine conversion method to attain the low power. In order to realize this objective , the design of 5-bit Gray counters and multiphase clock generator are careful for the multi-channel single ramp ADC to progress the devise performance methodology. Sampling rate improvement, the power analysis of the proposed and wilkinson ADC is shown in Table 1. Coarse and fine conversion methods are introduced in time-to-digital conversion (TDC) toward check the sampling rate and power analysis of the design.

Multiphase clock generator, includes the delay-locked loops (DLLs) for the fine conversion. The proposed ADC architecture consists of a ramp generator, a counter, a multiphase clock generator (MCG),a comparators, registers and encoders Single or array of DLL are used in the fine conversion. The block diagram of proposed ADC is shown in Fig.5. Intended for a multi-channel topology, the ramp generator and the counter are common by all channel. every channel consists of one comparator and registers.

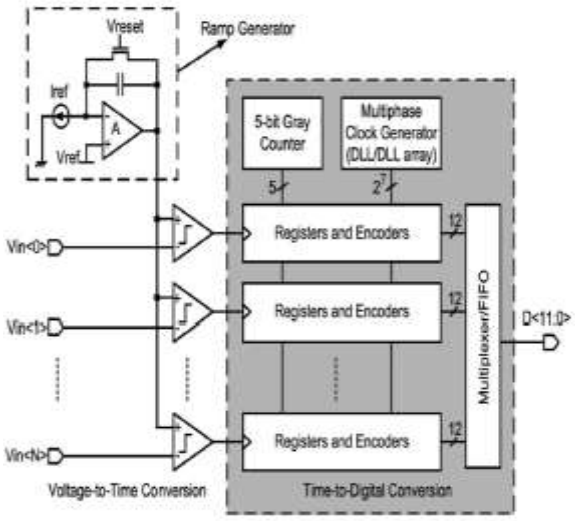


**Fig 5. Block diagram of proposed ADC with coarse and fine conversion**

In coarse conversion, 5-bit Gray counter is selected , which dissipates the low down power. Counter is restricted by the reset signa l, it is also used in the ramp generator. For fine conversion, multiphase clock generator (MCG) is fitting for the sampling purpose. In DLL, it is utilized to devise a time amplifier. The gain value be capable of exist automatic by any input of the integer value

**TABLE 1**

**PERFORMANCE COMPARISION OF WILKINSON AND MULTI-CHANNELADC**

| Performances | Wilkinson ADC | Multi-channel ADC |
|---|---|---|
| Number of bits | 11 | 12 |
| Sampling rate | 66.7KHz | 2.5MHz |
| Power | 6.5mW | 2.4mW |

## REFERENCES

[1] M.Ahmadi and W.Miller,[July 2009]"A delay generation technique for narrow time interval measurement,"IEEE Transactions on Istrumentation and Measurement.,vol. 58, no. 7, pp. 2245–2252.

[2] G.Bertuccio, F.Borghetti and S.Caccia ,[August 2007]"A complete read-out channel with embedded Wilkinson A/D converter for Xray spectrometry,"IEEETransactions on Nuclear Science.,vol.54,no.4,pp.1216–1221.

[3] J.Bouvier, M.Dahoumane,D.Dzahiniand J.Hostachy,[August 2007]"A low power and low signal 5-bit 25 MS/s pipelined ADC for monolithic active pixel sensors,"IEEE Transactions on Nuclear Science., vol. 54, no. 4, pp. 1195–1200.

[4] D.Breton, E.Delagnes, F. Lugiez and R. Rahmanifard,[October 2007]"A low power multi-channel single ramp ADC with up to 3.2 Ghz virtual clock," IEEE Transactios on Nuclear Science.,vol. 54, no. 5, pp. 1735-1742.

**[5]** J.Britton, M.Emery, S.Frank and A.Wintenberg,[June 1997]"A multi-channel ADC for use in the PHENIX detector," IEEE Transactions on Nuclear Science., vol. 44, no. 3, pp. 374–378.