ATTENDANCE SYSTEM USING NFC TECHNOLOGY AND EMBEDDED CAMERA DEVICE ON MOBILE PHONE

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ABSTRACT

This project proposes the design and development to create a system that makes easier to check students' attendance automatically, and this system is implemented in based on NFC technology. Registering for attendance in education environments especially universities is a highly demanding activity as a result of increasing number of students. The attendance process normally involves circulating a paper for the students to register their names, or the lecturer calling the names and registering the students either in a paper or from PDA/PC. In the first case the students' attention may be attracted while taking the lectures and at the same time they can register for students who do not being present in the class.

Keywords: NFC technology, NFC mobile application smart attendance system, wireless attendance system

I. INTRODUCTION

In the most of Thailand universities, instructors take attendance by calling out the names and surnames of students, and then marking them, while, in others, instructors pass around a sheet of paper, asking students to sign in attendance sheet just next to their surnames. Both practices have their drawbacks. In the first case, if numerous groups attend the lesson, checking all of these students by name and surname might take about several minutes out of each lesson; in the second case, friends of absent students may write down their names and surnames. These practices place university instructors and their institutions at considerable disadvantages when it comes to taking attendance. To rectify these systematic failings, we have desire to put the NFC tag into service. Each tag has a unique ID, precluding the duplication of a tag. These NFC tag are given to students of Apply Mathematic department, Faculty of and while students entering classrooms and touch these tag on instructor mobile phone, NFC readers program on instructor's mobile phone will read these tags, identify the students from their respective NFC tag and send the data to an instructor's mobile phone. Mobile phone, in turn, sends all the data it has collected to the server by the end of lesson, or at the end of this day according to the preference of lecturer. This means no class time will be wasted.

II. EXISTING SYSTEM

Currently Some universities prefer to use paper sheet for controlling attendance, whereas some universities prefer to use paper sheet for checking students' attendance and after this, fill out these information into a system manually.

III. PROPOSED SYSTEM

This paper propose to create a system with one server PC to which all NFC device are connected, so all data will be saved in one database on server PC and send to the database on the server too, making the monitoring of the information effortless. All instructors must have a NFC device with an embedded NFC reader that can read student NFC tag, as well as an embedded camera device on mobile phone that can take their photos. The camera device is meant to prevent a student from giving his/her NFC tag to a classmate who attends the lecture, touch the other student's NFC tag to make it appear as if s/he had also attended. When a student enters class and touch his/her NFC tag on instructor's mobile phone, the NFC reader reads his/her student NFC tag, while the camera device on mobile phone simultaneously takes his/her photo and sends it to the database in instructor's mobile phone.

After some time, the instructor submits all data for backup in a database server. When students enter the classroom and touch theirs NFC tag near instructor's NFC device the NFC reader on mobile phone automatically reads their NFC tag and the embedded camera device on takes their photos as NFC or near-field communication, is an easy and intuitive technology that allows user to use user's mobile phone for special purposes. An NFC tag can share and link to information such as web pages, social media and all other sorts of other information generally. Other areas where NFC is starting to evolve into are making payments, opening doors secured with contactless locks, logging on to computers and many more. All of these actions have something in common, that is they invoke an action based on user placing NFC device near (the N in NFC) the thing user want to read or interact with. NFC is bridging the gap between both the physical and virtual worlds. By bringing two devices near each other, there is a virtual reaction. Bluetooth and Wi-Fi do not have this ease in set up. So the key feature of NFC is automatic and there is no need to launch an MATLAB application.

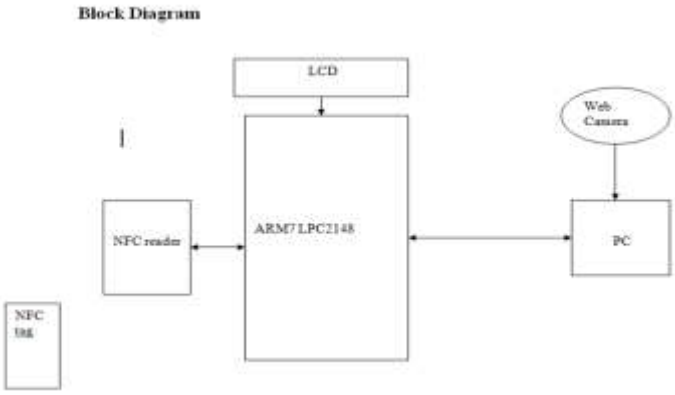


Figure 1: Block Diagram of Proposed Work

3.1 ARM 7

The LPC2141/2/4/6/8 microcontrollers are based on a 32/16 bit ARM7TDMI-S CPU with real-time emulation and embedded trace support, that combines the microcontroller with embedded high speed flash memory ranging from 32 kB to 512 kB. A 128-bit wide memory interface and unique accelerator architecture enable 32-bit code execution at the maximum clock rate. For critical code size applications, the alternative 16-bit Thumb mode reduces code by more than 30 % with minimal performance penalty. Due to their tiny size and low power consumption, LPC2141/2/4/6/8 are ideal for applications where miniaturization is a key requirement, such as access control and point-of-sale. A blend of serial communications interfaces ranging from a USB 2.0 Full Speed device, multiple UARTS, SPI, SSP to I2Cs and on-chip SRAM of 8 kB up to 40 kB, make these devices very well suited for communication gateways and protocol converters, soft modems, voice recognition and low

end imaging, providing both large buffer size and high processing power. Various 32-bit timers, single or dual 10-bit ADC(s), 10-bit DAC,

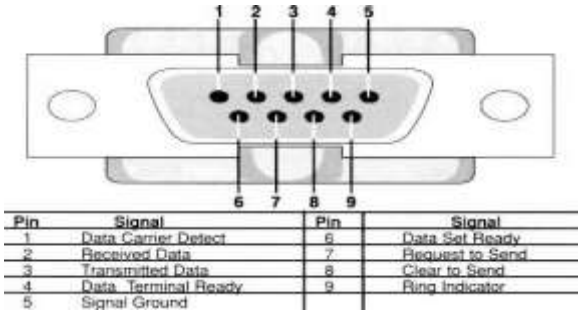
PWM channels and 45 fast GPIO lines with up to nine edge or level sensitive external interrupt pins make these microcontrollers particularly suitable for industrial control and medical systems. 16/32-bit ARM7TDMI-S microcontroller in a tiny LQFP64 package.

- ❖ 8 to 40 kB of on-chip static RAM and 32 to 512 kB of on-chip flash program memory. 128 bit wide interface/accelerator enables high speed 60 MHz operation.
- In-System/In-Application Programming (ISP/IAP) via on-chip boot-loader software.
- ❖ Single flash sector or full chip erase in 400 ms and programming of 256 bytes in 1 ms.
- ❖ EmbeddedICE RT and Embedded Trace interfaces offer real-time debugging with the on-chip RealMonitor software and high speed tracing of instruction execution.
- USB 2.0 Full Speed compliant Device Controller with 2 kB of endpoint RAM.
- ❖ In addition, the LPC2146/8 provide 8 kB of on-chip RAM accessible to USB by DMA.
- ❖ One or two (LPC2141/2 vs. LPC2144/6/8) 10-bit A/D converters provide a total of 6/14 analog inputs, with conversion times as low as 2.44 µs per channel.
- Single 10-bit D/A converter provides variable analog output.
- ❖ Two 32-bit timers/external event counters (with four capture and four compare channels each), PWM unit (six outputs) and watchdog.
- Low power real-time clock with independent power and dedicated 32 kHz clock input.
- ❖ Multiple serial interfaces including two UARTs (16C550), two Fast I2C-bus (400 kbit/s), SPI and SSP with buffering and variable data length capabilities.
- Vectored interrupt controller with configurable priorities and vector addresses.
- Up to 45 of 5 V tolerant fast general purpose I/O pins in a tiny LQFP64 package.
- ❖ Up to nine edge or level sensitive external interrupt pins available. 60 MHz maximum CPU clock available from programmable on-chip PLL with settling time of 100 µs.
- ❖ On-chip integrated oscillator operates with an external crystal in range from 1 MHz to 30 MHz and with an external oscillator up to 50 MHz.
- Power saving modes include Idle and Power-down.
- ❖ Individual enable/disable of peripheral functions as well as peripheral clock scaling for additional power optimization.
- Processor wake-up from Power-down mode via external interrupt, USB, Brown-Out
- ❖ Detect (BOD) or Real-Time Clock (RTC).
- Single power supply chip with Power-On Reset (POR) and BOD circuits:

– CPU operating voltage range of 3.0 V to 3.6 V (3.3 V ± 10 %) with 5 V tolerant I/O

Figure 2: ARM Processor

An RS-232 serial port was once a standard feature of a personal computer, used for connections to modems, printers, mice, data storage, uninterruptible power supplies, and other peripheral devices. However, RS-232 is hampered by low transmission speed, large voltage swing, and large standard connectors. In modern personal computers, USB has displaced RS-232 from most of its peripheral interface roles. Many computers do not come equipped with RS-232 ports and must use either an external USB-to-RS-232 converter or an internal expansion card with one or more serial ports to connect to RS-232 peripherals. RS-232 devices are widely used, especially in industrial machines, networking equipment and scientific instruments.



Pin	Signal	Pin	Signal
1	Data Carrier Detect	6	Data Set Ready
2	Received Data	7	Request to Send
3	Transmitted Data	8	Clear to Send
4	Data Terminal Ready	9	Ring Indicator
5	Signal Ground		

Figure 3: Serial Port

IV. CONCLUSION

The system presented in this project will substantially improve the current day's attendance registration system and eliminate many paper works involved in it. Other benefits include eliminating the chance of losing attendance data, different attendance reports can be easily generated by a click of mouse, simplifying the decision making process related to attendance, etc. One of the major distinct characteristics of our proposed system is that the hardware required is minimal, i.e. Only NFC tag and NFC-enabled mobile device.

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