BINARY ADDERS TO IMPROVE ENERGY EFFICIENT USING QUANTUM DOT CELLULAR AUTOMATA

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ABSTRACT

As transistors decrease in size more and more of them can be accommodated in a single die, thus increasing chip computational capabilities. However, transistors cannot get much smaller than their current size. The quantum-dot cellular automata (QCA) approach represents one of the possible solutions in overcoming this physical limit, even though the design of logic modules in QCA is not always straightforward. Many logical circuits are designed using QCA which consume low power. Designing of adders using QCA. Increase on number of new results on adders. To design adders and detailed simulation using QCAD designer. The performance is increased by adder. Delay performance compared to Ripple carry adder (RCA).

Keywords: QCA CELL, RCA Adder

I. INTRODUCTION

Quantum Dot cellular Automata (QCA) don't use transistors. Basic element of QCA is a quantum cell; each quantum cell has electrons in them. Electron transmission occurs on the columbic interaction of the electrons. QCA encodes binary information in the charge configuration within a cell. QCA is an advanced research program and efforts are made to reduce the complexity of the circuits. In this brief, an innovative technique is presented to implement high-speed low-area adders in QCA. Theoretical formulations demonstrated for CLA and parallel-prefix adders are here exploited for the realization of a novel 2-bit addition slice. The latter allows the carry to be propagated through two subsequent bit-positions with the delay of just one majority gate (MG). In addition, the clever top level architecture leads to very compact layouts, thus avoiding unnecessary clock phases due to long interconnections.

II. QCA CELL

A quantum-dot cellular automata (QCA) is a square nanostructure of electron wells having free electrons. Each cell has four quantum dots. The four dots are located in the four corners. The cell can be charged with two free electrons.

Logic 0 logic 1

A QCA is a nanostructure having as its basic cell a square four quantum dots structure charged with two free electrons able to tunnel through the dots within the cell. Because of Columbic repulsion, the two electrons will always reside in opposite corners. The locations of the electrons in the cell (also named polarizations P) determine two possible stable states that can be associated to the binary states 1 and 0.

Even though these addition circuits use different topologies of the generic FA, they have a carry-in to carry-out path consisting of one MG, and a carry-in to sum bit path containing two MGs plus one inverter. As a consequence, the worst case computational paths of the n-bit RCA and the n-bit CFA consist of (n+2) MGs and one inverter.

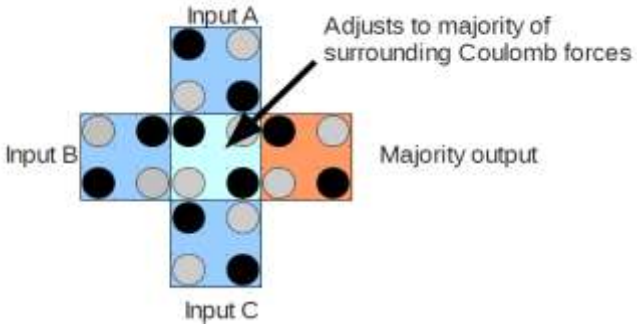

Figure 1: QCA Majority Voter

In particular, the auxiliary propagate and generate signals, namely pi = ai + bi and gi = ai · bi , are computed for each bit of the operands and then they re grouped four by four. Such a designed n-bit CLA has a computational path composed of 7+4×(log4 n) cascaded MGs and one inverter. This can be easily verified by observing that, given the propagate and generate signals (for which only one MG is required), to compute grouped propagate and grouped generate signals; four cascaded MGs are introduced in the computational path. In addition, to compute the carry signals, one level of the CLA logic is required for each factor of four in the operands word-length. This means that, to process nbit addends, log4 n levels of CLA logic are required, each contributing to the computational path with four cascaded MGs. When n-bit operands are processed, its worst case computational path consists of 4×log2 n−3 cascaded MGs and one inverter. Apart from the level required to compute propagate and generate signals, the prefix tree consists of 2 × log2n − 2 stages.

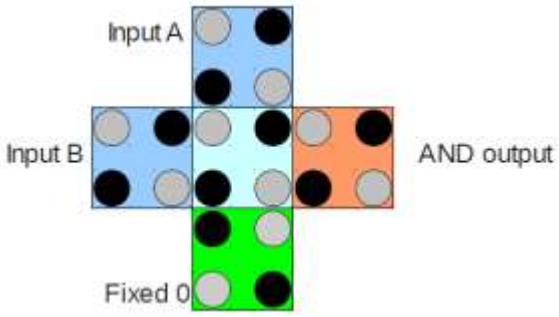

Figure 2: And Gate

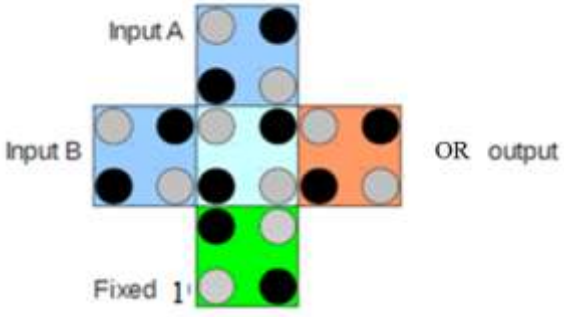

Figure 3: Or Gate

To introduce the novel architecture proposed for implementing ripple adders in QCA, let consider two n-bit addends A = an−1. . . a0 and B = bn−1. . . b0 and suppose that for the i th bit position (with i = n − 1. . . 0) the auxiliary propagate and generate signals, namely pi = ai + bi and gi = ai · bi , are computed. ci being the carry produced at the generic (i−1)th bit position, the carry signal ci+2, furnished at the (i+1)th bit position, can be

computed using the conventional CLA logic reported. In this way, the RCA action, needed to propagate the carry ci through the two subsequent bit positions, requires only one MG.

Conversely, conventional circuits operating in the RCA fashion, namely the RCA and the CFA, require two cascaded MGs to perform the same operation. In other words, an RCA adder designed as proposed has a worst case path almost halved with respect to the conventional RCA and CFA.

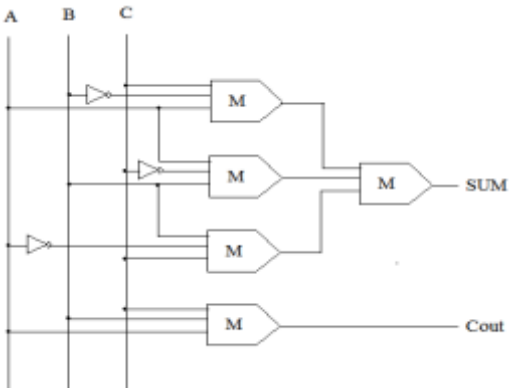

Figure 4: Conventional Adder

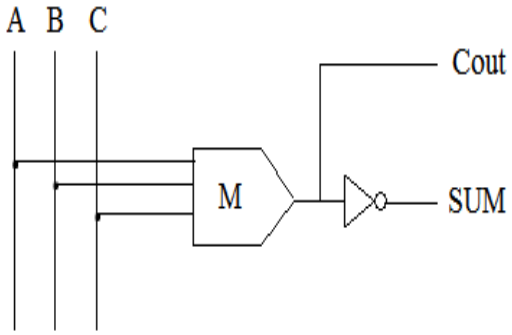

Figure 5: Conventional Adder

III. RESULTS AND DISCUSSION

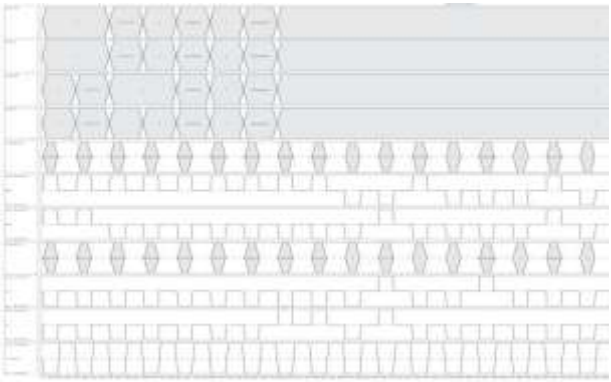

Figure 5: Adder with 64 bit

IV. CONCLUSION

A new adder designed in QCA was presented. It achieved speed performances higher than all the existing QCA adders, with an area requirement comparable with the cheap RCA and CFA demonstrated. The novel adder operated in the RCA fashion, but it could propagate a carry signal through a number of cascaded MGs significantly lower than conventional RCA adders. In addition, because of the adopted basic logic and layout strategy, the number of clock cycles required for completing the elaboration was limited. A 64-bit binary adder designed as described in this brief exhibited a delay of only nine clock cycles, occupied an active area of 19.72 μm2, and achieved an ADP of only 169.48.

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