DESIGN MOFET BASED TRANSMITTER FOR ONCHIP INTERCONNECTS

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ABSTRACT

The growing demand for wide bandwidth communication in a serial link transceiver within the integrated circuits calls for large number of high speed inputs and outputs per chip. In serial link transceiver propose various techniques to achieve low swing signals. These techniques are used to transmit the signals through interconnects using different types of drivers and receivers. Objective of this work is design a driver circuit in transmitter using MOSFET. The proposed transmitter achieves less delay compare to repeater insertion method. In driver circuit both current mode and voltage mode multiplexers are used to drive on-chip global interconnects. In voltage mode multiplexer consumes less power than current mode. But current mode has less delay, low swing and achieves wide bandwidth. In this work illustrates current mode driver and to implement some low swing techniques to compare the results such as power, delay, energy, swing, bandwidth. The low swing techniques are Conventional Level Converter (CLC) and Symmetric Source Follower Driver with Level Converter (SSDLC). The proposed transmitter implemented using 180nm technology through simulation with Synopsys HSPICE.

Keywords: Low Swing, Voltage Mode Driver, Current Mode Driver

I. INTRODUCTION

In transmitter circuit both voltage and current mode techniques are used to transmit the signals. In order to achieve low swing and propagation delay we propose pseudo NMOS multiplexing based current mode driver and also to implement some low swing techniques. The low swing techniques are conventional level converter and symmetric source follower with level converter. In that proposed techniques driven by a factor of two compare to that using repeater insertion techniques. Transmitter circuit implemented by Hspice simulator using 180nm technology.

II. SIGNALLING TECHNIQUES

Depending upon the physical arrangement of the wire channels of data links, electrical signaling schemes for data transmission over wire channels can be classified into single ended, fully differential. In an effort to reduce the intrusion of repeater logic, reduce power dissipation, and potentially drive longer distances, differential low swing signaling may be employed. They can also be categorized into voltage mode and current mode signaling schemes on the basis of the carriers of data links.

2.1 Voltage Mode Signalling

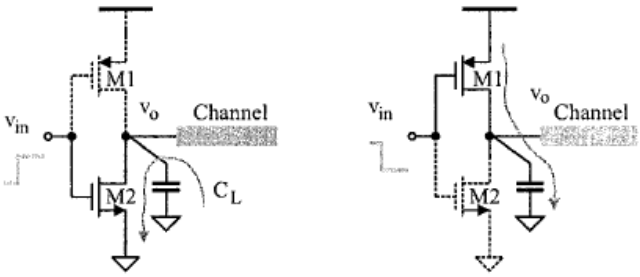

Fig 2.1 Voltage Mode Signaling.

The signal conveyed to the channel by the driver is the output voltage of the inverter. It is determined from

$$C_L \frac{dv_o(t)}{dt} + \frac{dv_o(t)-V_{DD}}{R_p} - C_L V_{OL}\partial(t) = 0 \quad (Risingedge) \qquad (2.1)$$

$$C_L \frac{dv_o(t)}{dt} - C_L V_{OH}\partial(t) + \frac{dv_o(t)}{R_n} = 0 \quad (Fallingedge) \qquad (2.2)$$

where *Rn* and *Rp* are the channel resistance of the NMOS and PMOS transistors in the triode, respectively, *CL* is the load capacitance of the driver, *VOL and VOH* are the voltage of Logic-0 and Logic-1 states, respectively, $C_L V_{OL}\partial(t) and C_L V_{OH}\partial(t)$quantify the effect of the initial voltage of the load capacitor at the onset of charging and discharging.

2.2 Current Mode Signaling

Current mode signaling offers the advantages of low supply voltage requirement, a small propagation delay, superior signal integrity, low switching noise, and low power consumption. The single-ended signaling scheme cannot reject the noise coupled to the channels. In addition, the channels of data links with single ended signaling have a large inductance and are sensitive to inductive interferences from other sources.

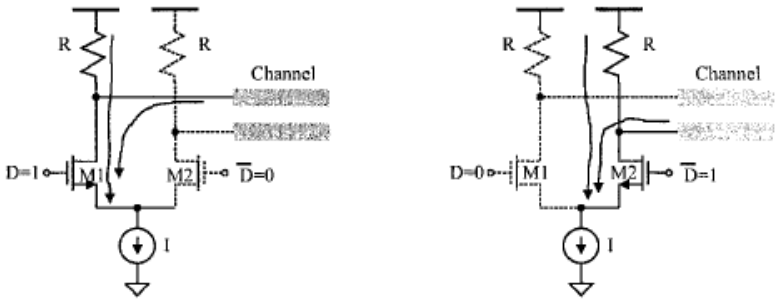

Fig 2.2 Current Mode Signaling.

Fully differential signaling effectively rejects the noise coupled to the channels at the cost of two conductors per channel. Data links with fully differential signaling have a small channel inductance and a low electromagnetic emission. At the receiver side, together with the drawback of voltage-mode signaling, limit data rates. Current

mode incremental signaling, on the other hand, achieves high data rates by utilizing the advantages of the fully differential and current mode signaling schemes. Data links with current mode incremental signaling have a small channel inductance and a low level of electromagnetic emission.

III. DRIVER (TRANSMITTER) CIRCUITS

A transmitter circuit encodes a symbol in to current or voltage for transmission over a line. A good transmitter for driving interconnects has output impedance optimized for selected transmission mode.

3.1 Voltage Mode Driver

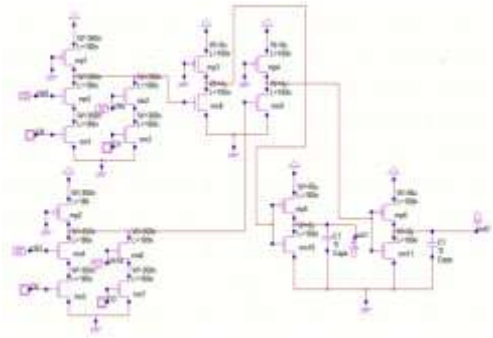

Fig.3.1 Voltage Mode Driver

Transmitter consists of multiplexer, predriver, output driver. The transmitter multiplexes parallel data (D0-D3) generates differential serial data output and drives it to interconnect segment. Pseudo NMOS voltage mode multiplexer requires only one driver for all the inputs. Input data and depending on the selected line the output to be high. The signal is driven by the predriver. Predriver nothing but static inverter used to reduce the output delay and convert full swing signal into limited signal. Finally Output Driver to reduce the swing and reducing power consumption. In Voltage mode driver the capacitor is charging and discharging the signal value is 1F. Similarly the complement signal is generated using the complemented data inputs to output.

3.2 Current Mode Driver

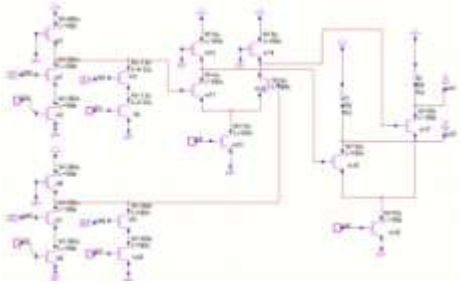

Fig. 3.2 Current Mode Driver

The large size of MOS voltage mode drivers and the large amount of delay and energy consumed by the required predrivers are a significant disadvantage of voltage mode signalling. The current mode drivers are significantly faster and more power efficient than low impedance voltage mode driver. So to reduce output delay, current steering driver should be used with limited swing predriver. It consists of a 4 : 1 multiplexer, a

preamplifier, and an output driver. The transmitter employs dual pseudo NMOS multiplexers at its input, one for the signal and one for its complement. Each multiplexer input is switched by two series NMOS that are gated by two adjacent clock phases in the same manner that the driver pull downs are gated by adjacent clock phases.

3.3 Conventional Level Converter (CLC)

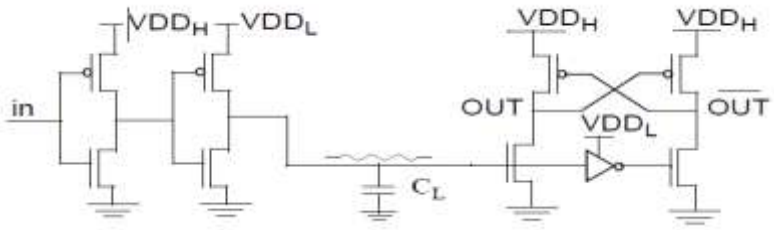

Fig. 3.3 Conventional Level Converter

The driver uses an extra supply with lower voltage to drive the interconnect from 0 to VDDL. The receiver is actually a differential amplifier, with an internal inverter to generate a complementary input signal. This circuit achieves a quadratic energy saving on the interconnect, proportional to VDDL 2.Moreover, VDDL should be large enough to ensure a reasonable noise margin. With VDDH=2.0V, the optimal VDDL for minimum energy delay product is 1.1V, which reduces the overall energy to 40% of that of full swing circuit.

3.4 Symmetric Source Follower with Level Converter (Ssdlc)

The circuit of **SSDLC** scheme is shown in Fig.3.4. The driver drives the interconnect with an output swing from Vtn to Vdd- Vtn, shown as node *in2* in Fig.3.4. The threshold voltages are subject to the body effects. The basic idea of the symmetric level converter is similar to the one in Hitachi circuit.

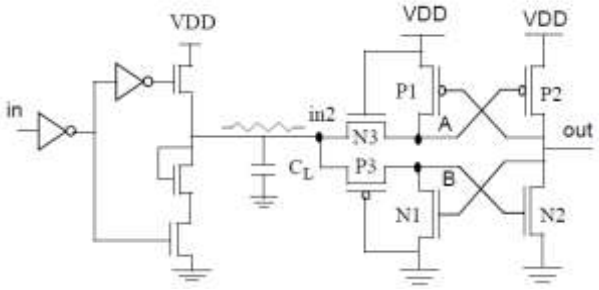

Fig.3.4 Symmetric Source Follower Driver with Level Converter

IV. PERFORMANCE CHARACTERISTICS

Table 4.1 Performance Characteristics in avg, peak power, delay

SCHEME	AVG POWER	PEAK POWER	DELAY
VOLTAGE MODE	1.0922E-02	1.4507E-02	2.7351E-10
CML	2.3155E-02	2.4911E-02	1.872E-10
CLC	2.8255E-04	2.1975E-03	5.9459E-10
SSDLC	9.9197E-04	3.7262E-03	1.1097E-10

Table 4.1 shows that comparison of average, peak power, and delay. Compare to voltage mode, the current mode logic consume more power but delay reduced. In order to reduce the power CLC and SSDLC techniques to be used.

Table 4.2 Performance characteristics in swing, energy, and rise time fall time

SCHEME	SWING	ENERGY	RISE & FALL TIME
VOLTAGE MODE	1.8037	1.0803E-10	2.0102E-10 & 1.8173E-10
CML	1.0914	2.2922E-10	1.6737E-10 & 1.6737E-10
CLC	1.9003	1.7443E-12	8.8059E-11 & 2.9731E-10
SSDLC	7.3711E-01	5.8785E-12	-

Table 4.2 shows that comparison of Swing, energy, rise and fall time. Compare to CLC, voltage mode, CML, SSDLC achieve less swing. Less energy achieved by CLC and SSDLC. In SSDLC technique cannot measure rise and fall time because of output goes to low state.

V. CONCLUSION

In this work, the differential current mode transmitter for on-chip serial interconnect using pseudo NMOS logic based multiplexer has been proposed. To implement current mode to achieve low swing and delay can be reduced but consumed more power than to voltage mode. So in order to reduce the power, two low swing techniques has been proposed. In summary reducing the swing on interconnect is an effective & powerfull tool for the minimization of energy dissipation but requires a judicious optimization with respect to robustness, design complexity and energy dissipation. As a future, MOSFET has high leakage current due to scaling of transistor at below 32nm technology. So to reduce the leakage current propose CNTFET based transmitter for both voltage mode, current mode driver and to compare the results.

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BIOGRAPHICAL NOTES

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