FAULT CURRENT LIMITER IN SINGLE PHASE AND THREE PHASE LINES FOR COMPENSATING VOLTAGE SAG

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ABSTRACT

Potential fault current levels in power grids is approaching, and may eventually exceed, the short-circuit-current limits of existing protection devices. Alternative to expensive system upgrades of protection devices, Fault Current Limiters (FCL's) provide more cost-effective solutions to prevent old protection devices and other equipment on the system from being damaged by excessive fault currents. Short circuit faults are often the origin of voltage sags at a point of common coupling (PCC) in a power network, the extent of the voltage sag is proportional to the short circuit current level, reducing the fault current level within the networks can reduce voltage sags during faults and protect sensitive loads that are connected to the same PCC. The proposed structure prevents voltage sag and phase-angle jump of the substation PCC after fault occurrence. As a result, other feeders, which are connected to the substation PCC, will have good power quality. In this paper a three phase fault current limiter is proposed. A Matlab/Simulink model is developed and simulation results are presented. Finally the simulation results are validated through experimentation.

Keywords - Fault Current Limiter (FCL), Point Of Common Coupling (PCC), Power Quality (PQ), Semiconductor Switch, Total Harmonic Distortion (THD), And Voltage Sag.

I. INTRODUCTION

Power quality variations are classified as either disturbances or steady state variations. Disturbances pertain to abnormalities in the system voltages or currents due to fault or some abnormal operations. Steady state variations refer to rms deviations from the nominal quantities or harmonics. In general these are monitored by disturbance analyzers, voltage recorders, harmonic analyzers etc. However with the advancement in the computer technology, better, faster and more accurate instruments can now be designed for power quality monitoring and analysis.

The input data for any power quality monitoring device is obtained through transducers. These include current transformers, voltage transformers, Hall-effect current and voltage transducers etc. Disturbance analyzers and disturbance monitors are instruments that are specifically designed for power quality measurements. There are two categories of these devices - conventional analyzers and graphics-based analyzers.

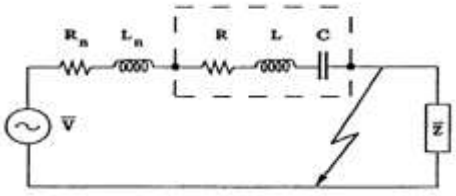
Conventional analyzers provide information like magnitude and duration of sag/swells, under/over voltages etc. Graphic-based analyzers are equipped with memory such that the real-time data can be saved. The advantage of this device is that the saved data can be analyzed later to determine the source and cause of the power quality problems.

Voltage sag is an important PQ problem because of sensitive loads growth. Worldwide experience has show that short-circuit faults are the main origin of voltage sags and, therefore, there is a loss of voltage quality. This problem appears especially in buses which are connected to radial feeders [1]–[6]. Faults at either the transmission or distribution level may cause transient voltage sag or swell in the entire system or a large part of it. Also, under heavy load conditions, a significant voltage drop may occur in the system. Voltage sags can occur at any instant of time, with amplitudes ranging from 10–90% and a duration lasting for half a cycle to one minute. Further, they could be either balanced or unbalanced, depending on the type of fault and they could have unpredictable magnitudes, depending on factors such as distance from the fault and the transformer connections. Voltage swell, on the other hand, is defined as a sudden increasing of supply voltage up 110% to 180% in RMS voltage at the network fundamental frequency with duration from 10 ms to 1 minute.

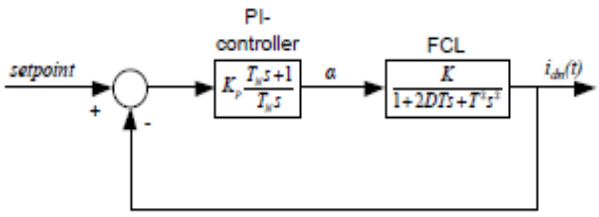
Voltage swells are not as important as voltage sags because they are less common in distribution systems. Voltage sag and swell can cause sensitive equipment (such as found in semiconductor or chemical plants) to fail, or shutdown, as well as create a large current unbalance that could blow fuses or trip breakers. The voltage sag during the fault is proportional to the short-circuit current value. An effective approach to prevent expected voltage sag and improve the voltage quality of point of common coupling (PCC) is fault current limitation by means of a device connected at the beginning of most exposed radial feeders [9].

II. BASIC FCL

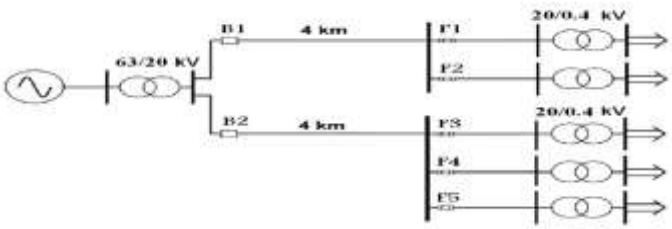
For a highly reliable power supply, the fault current limiter (FCL) is becoming an essential part in modern power systems. The current-limiting device is required to be introduced into the power system to prevent the fault current from rising to its full prospective value.



(a).Basic FCL principle scheme



(b) Shows the control structure of the FCL



(c) Test System

Fig.1: Representation of Basic FCL System.

This can also be attributed to the concern over power quality (PQ) as FCLs can be used to mitigate voltage sags caused by faults. These will avoid upgrading switchgears during system expansion and improve the PQ delivered to customers. FCLs are needed to provide a limited and sustained short-circuit current through the fault for a sufficient time (e.g., 1 s) to enable proper coordination of protective relays in the overall protection scheme.

An ideal FCL should have the following characteristics:

- Zero resistance/impedance at normal operation;
- No power loss in normal operation and fault cases;
- Large impedance in fault conditions;
- Quick appearance of impedance when fault occurs;
- Fast recovery after fault removal;
- Reliable current limitation at defined fault current;
- Good reliability;
- Low cost.

III. PROPOSED FCL CONFIGURATION AND ITS OPERATION

Figure 2 shows the circuit topology of the proposed FCL which is composed of the two following parts:

1) Bridge part that includes a diode rectifier bridge, a small dc limiting reactor (L_{dc}). (Note that its resistance (R_{dc}) is involved too.), a semiconductor switch (IGBT or GTO), and a freewheeling diode (D_5).

2) Shunt branch as a compensator that consists of a resistor and an inductor ($R_{sh} + i\omega L_{sh}$).

Previously introduced structures for this application [4], [16], [17] have used two numbers of thyristors at bridge branches instead of one semiconductor switch inside the bridge (dc current route). Therefore, first, they have the more complicated control system. Second, in those structures, because of thyristors' operation delay (turn off at the first zero crossing), L_{dc} has a large value to limit the fault current between the fault occurrence instant and thyristors turn off instant, properly.

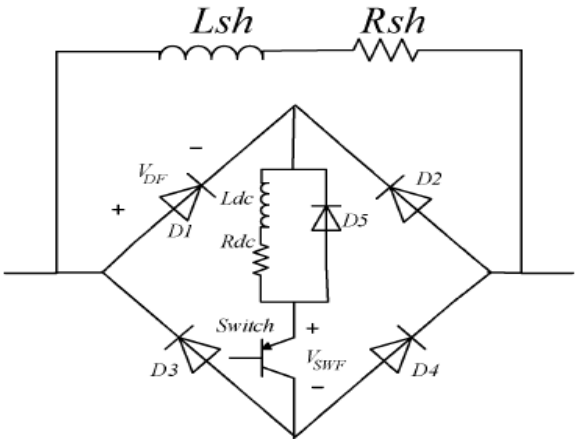


Fig.2: Proposed FCL Topology

This large value of L_{dc} leads to a considerable voltage drop on the FCL and the power losses including ac power losses on the shunt branch impedance and dc reactor power losses (if it is non superconductor) in the normal

condition. By using the semiconductor switch in the proposed structure and its fast operation, it is possible to choose a small value for L_{dc} to prevent severe di/dt at the beginning of the fault occurrence. So the voltage drop and power losses will be negligible. These days, high rating semiconductor switches are available in practice. However, using a self turn-off switch instead of thyristors in the proposed structure leads to higher cost [19]–[21]. From a power-loss point of view, in the normal condition, the proposed FCL has the losses on the rectifier bridge diodes, the semiconductor switch, and R_{dc}. Each diode of the rectifier bridge is ON in half a cycle, while the semiconductor switch is always ON. Therefore, the power losses of this FCL in the normal operation can be calculated as

$$\mathbf{P_{loss} = P_R + P_D + P_{SW}}$$

$$\mathbf{= R_{dc} I_{dc}^2 + 4V_{DF} I_{ave} + V_{SWF} I_{dc}}$$

Where,

I_{dc} dc side current which is equal to the peak of line current;

V_{DF} forward voltages drop on each diode;

V_{SWF} forward voltages drop on the semiconductor switch;

I_{ave} average of diodes current in each cycle that is equal to I_{peak}/π .

Considering (9) and the small value of dc reactor in this structure, the total power losses of the proposed structure become a very small percentage of the feeder's transmitted power. For example, by considering Table I parameters in the simulation section, the power losses will be 0.47% of the feeder's transmitted power.

On the other hand, in the fault condition, the PCC voltage drops on the shunt impedance. Therefore, the line current will pass through the shunt resistor (R_{sh}). As a result, power loss on the R_{sh} depends on its value that will be discussed in design considerations section. Note that the fault condition is several cycles and it is a small time interval.

Table-I

System Parameters

Source Side Data	Power Source	20kV, 50Hz, X/R ratio: 5 Total impedance: 1.608 Ω
	Transformer	20kV/6.6kV, 10MVA, 0.1pu
Distribution Feeders Data	Feeder F1	j0.314 Ω
	Feeder F2	j0.157 Ω
FCL Data	DC Side	L_{dc} = 0.01H, R_{dc} = 0.03 Ω V_{DF} = 3V, V_{SWF} = 3V, I_m = 0.6kA Switch type: IGBT
	Shunt Branch	L_{sh} = 0.08H, R_{sh} = 5 Ω
Load Data	Sensitive Load	10+j5.7 Ω
	Load of F2	15+j31.4 Ω

3.1 FCL in Distribution Network

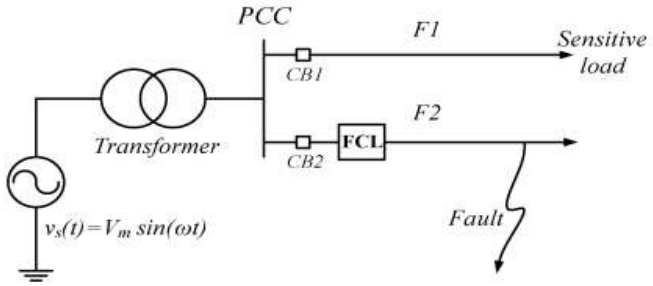


Fig.3: Single-line diagram of the power system

Fig.3: shows the single-line diagram of the power system. This figure shows a substation with only two feeders F1 and F2. However, the presented analysis can be easily extended to any number of feeders; The F1 supplies a sensitive load. With a fault in the F2, the voltage sag occurs in the substation PCC.

3.2 Hardware Schematic Diagram

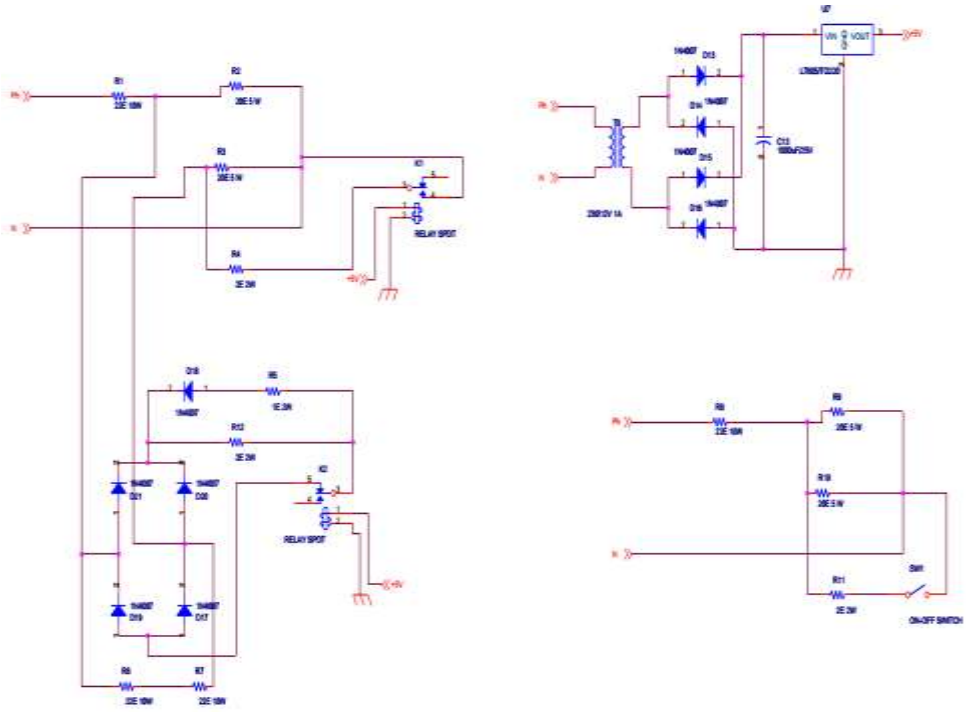


Fig.4: Hardware Schematic Diagram Circuit

IV. SIMULATION RESULTS

Case 1: Single Phase System.

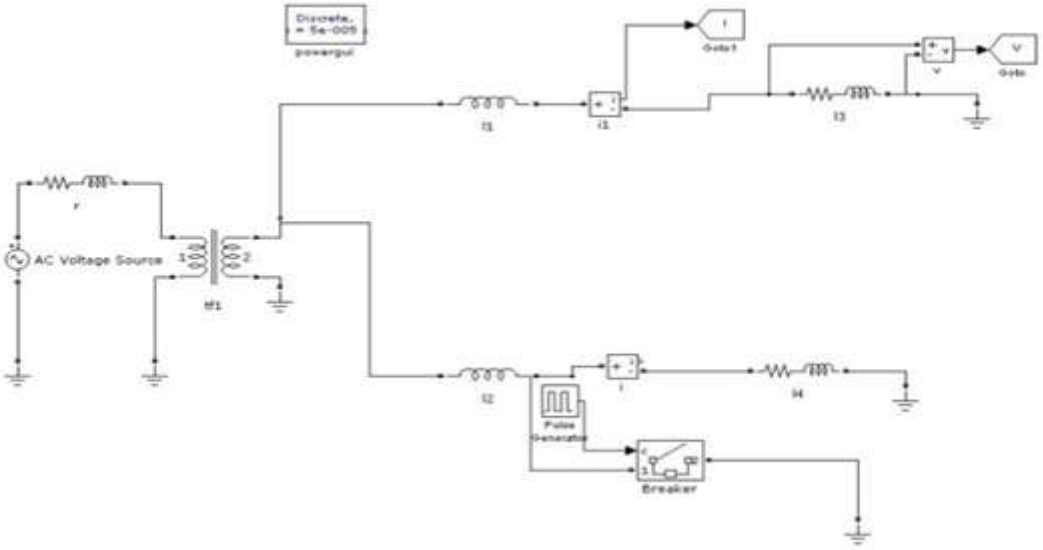


Fig.5: Simulink circuit of PCC without FCL

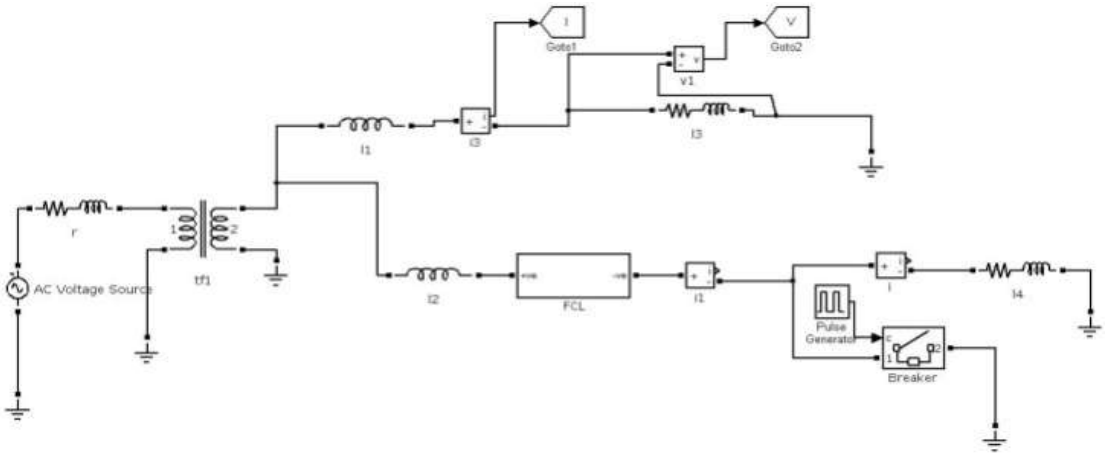


Fig.6: MATLAB/Simulink of the proposed circuit

Figure 5 and 6 shows the single phase power without and with FCL.

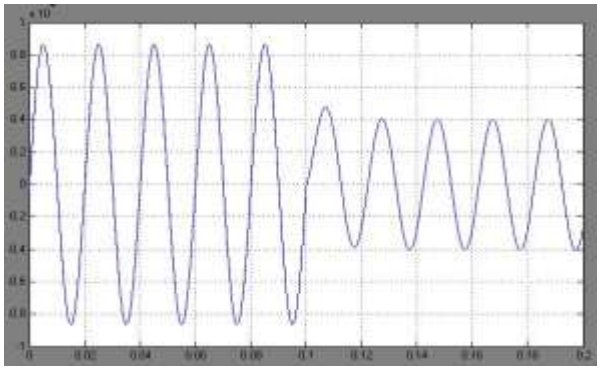


Fig.7: PCC Voltage without FCL

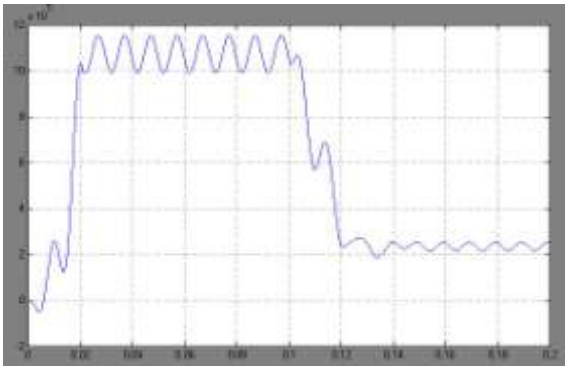


Fig.8: Single-phase instantaneous power of the sensitive load without FCL

Fig.7 shows the single phase voltage at PCC without the FCL. Fig.8 shows the single phase instantaneous power of the sensitive load which has reduced instantaneously after the fault has occurred.

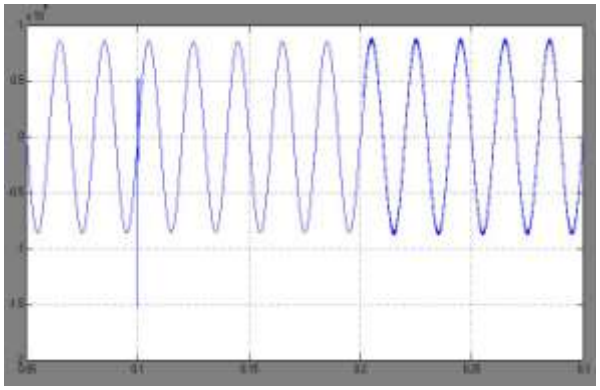


Fig.9: PCC voltage with the proposed FCL.

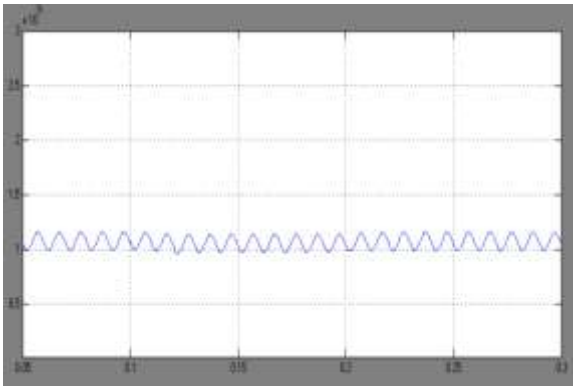


Fig.10: Single-phase instantaneous power of the sensitive load with the proposed FCL.

Fig.9. shows the single phase voltage at PCC with the FCL. It is found to be un distorted even a fault has occurred. Fig.10. shows the Single-phase instantaneous power of the sensitive load with the proposed FCL. It is seen that the power is remains unaltered during the fault. Fig.11. shows the voltage drop on the FCL during the fault. This voltage drop does not allow the PCC voltage to change.

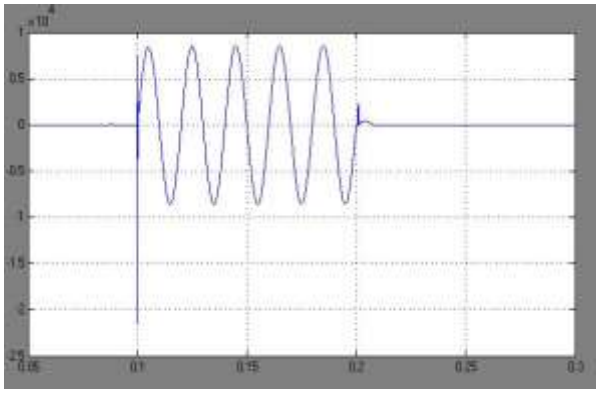


Fig.11: Voltage drops on the proposed FCL during impedance currents.

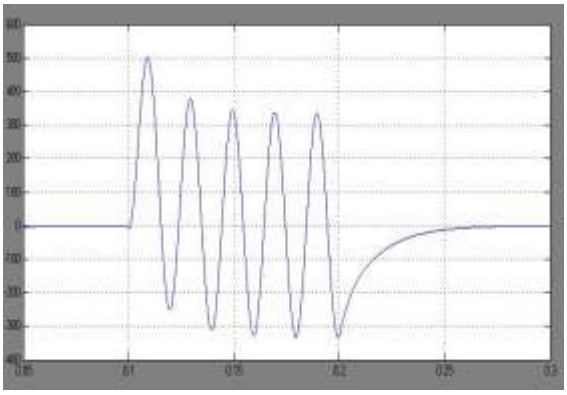


Fig.12: Line, dc reactor, and shunt Fault.

Fig.12. shows the shunt impedance current of the single phase system.

Case 2: Proposal of Three Phases FCL

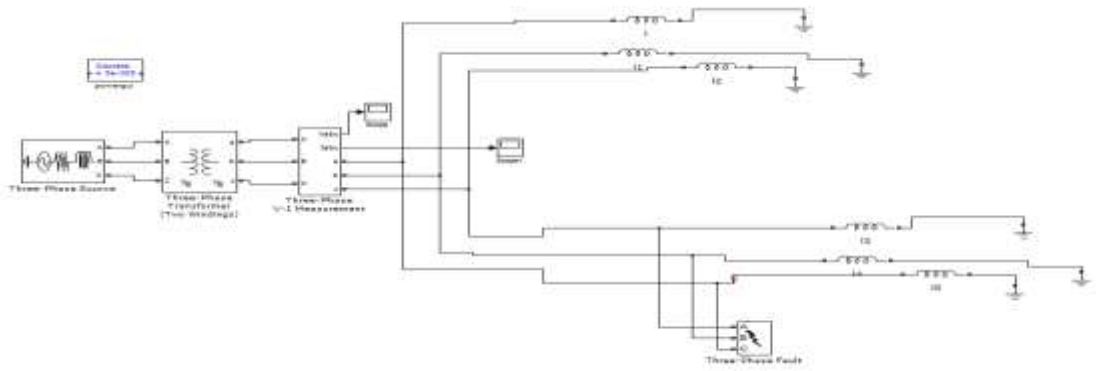


Fig.13: Simulink circuit of PCC without FCL

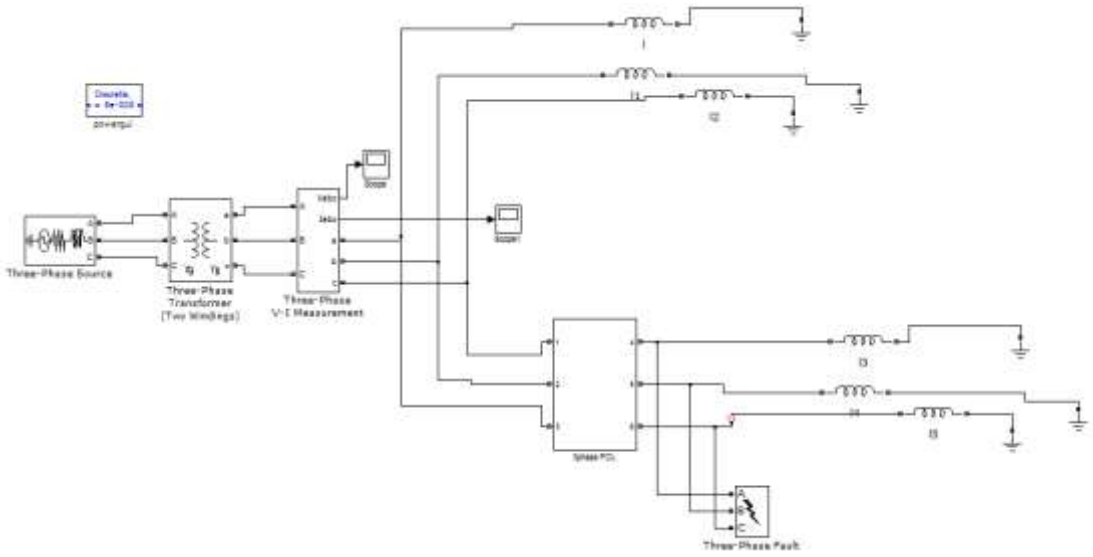


Fig.14: MATLAB/Simulink of the proposed circuit

Fig.13. and 14 shows the three phase power without and with FCL. Fig.15. shows the three phase voltage at PCC without the FCL

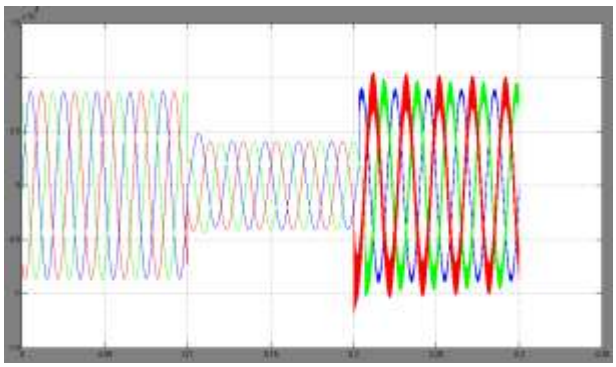


Fig.15: PCC Voltage without FCL

Fig.16: Three-phase instantaneous power of the sensitive load without FCL

Figure.16 shows the three phase instantaneous power of the sensitive load which has fallen instantaneously after the fault has occurred and recovered after the fault has cleared.

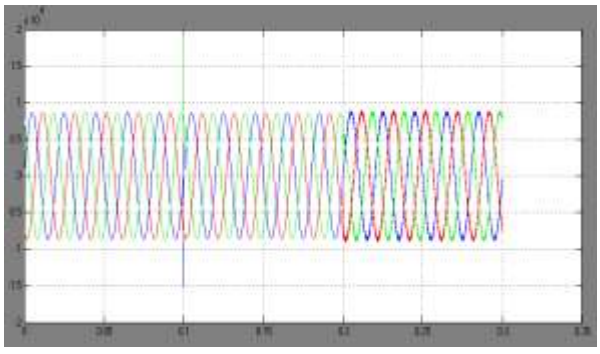


Fig.17: Three phase PCC voltage with the proposed FCL.

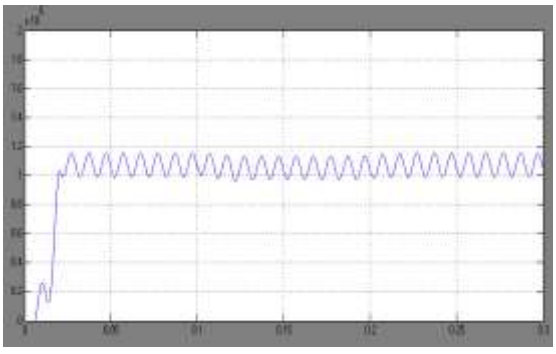


Fig. 18: Three-phase instantaneous power of the sensitive load with the proposed FCL.

Fig.17. show the three phase voltage at PCC with the FCL. It is found to be undistorted voltage waveform even a fault has occurred. Fig.18. shows the three-phase instantaneous power of the sensitive load with the proposed FCL. It is seen that the power is remains unaltered during the fault.

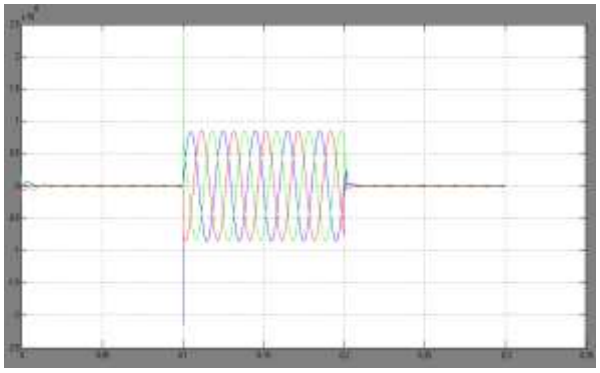


Fig.19: Three phase Voltage drop on the proposed FCL

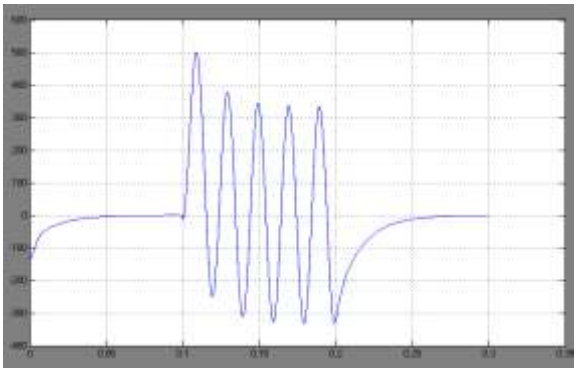


Fig.20:Line, dc reactor, and shunt impedance Currents during fault.

Fig.19. shows the three phase voltage drop on the FCL during the fault. This voltage drop does not allow the PCC voltage to change. Fig.20. shows the shunt impedance current for the three phase system.

Case 3: Hardware Implementation of single Phase FCL

Fig.21: Hardware circuit for single phase FCL

The proposed Fault current limiter is implemented in hardware at a low voltage level and the circuit behavior is analyzed. The input voltage used is 12V and to simulate a fault, we used a 5V DC relay. The relay is powered by using a L7805 voltage regulator. Two conditions of the circuit have been tested. One without fault current limiter and the other one is with fault current limiter.

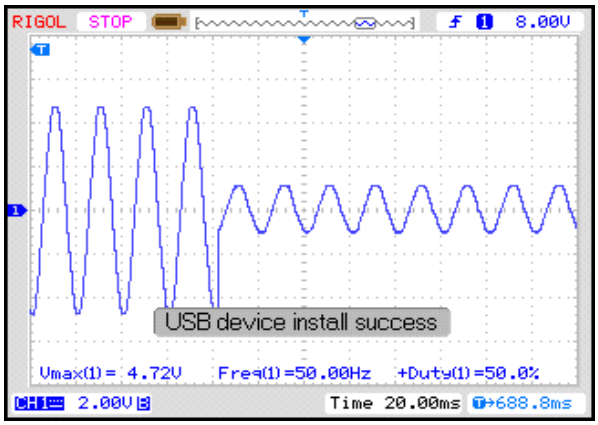


Fig.22: Voltage at PCC without FCL

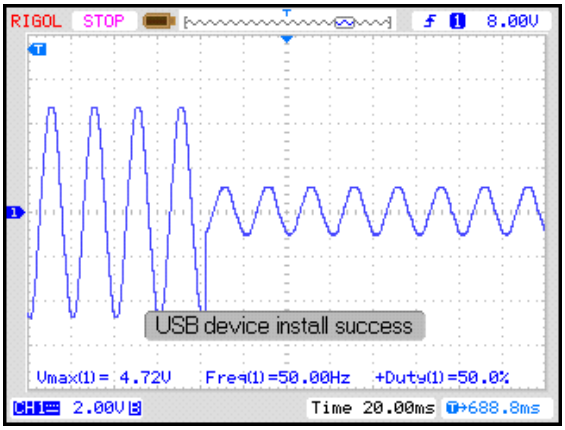


Fig. 23: Voltage at PCC with FCL.

As you can see in Figure 22, when there is a fault occurrence the voltage magnitude has been dropped down. In this Figure 23 we can see that when there is a fault occurrence the magnitude of the voltage does not change.

V. CONCLUSION

In this paper, by changing the previous circuit configuration the proposed FCL structure is introduced for voltage sag compensation, phase-angle jump mitigation, and fault current limiting operation due to the control method were analyzed. In this configuration the diodes will be in conduction only when fault occurs so, in normal condition current conducts through the switch by eliminating the diode losses in normal operating conditions. The proposed FCL has high speed. Note that the control system of this structure is simpler than previous ones. In addition, the dc voltage source placed in the proposed FCL structure reduces its THD and ac losses in normal operation. In general, this type of FCL, with the simple control circuit and low cost, is useful for the voltage-quality improvement because of voltage sag and phase-angle jump mitigating and low harmonic distortion in distribution systems. In addition to that the FCL is developed for the three phase power system. Their behaviors with and without the FCL are observed using Simulink results. Finally the simulation results are validated through experimentation.

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