AN EFFICIENT H-BRIDGE MULTILEVEL INVERTER FOR SPWM SCHEME OF AC MACHINE

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ABSTRACT

Induction Motor Direct Torque Control DTC is Earlier developed projects have pointed out the boundaries of conventional inverters, mainly in high-voltage and high-power requirements. In present years, multilevel inverters are smart and increasingly popular for high-power applications owing to their improved harmonic profile arrangement and augmented power ratings. Several implementations have been described in the literature on multilevel inverters technologies, control strategies, and applications. Conversely, there are few studies that really deliberate or evaluate the reliability and performance of induction motor drives connected by three-phase multilevel inverter. This paper implements a comparison approachment for a cascaded H-bridge multilevel inverter with direct torque control (DTC) for induction motor drive. In this circumstance, symmetrical and asymmetrical provisions of five-level and seven-level H-bridge inverters are implemented and compared in order to determine an optimum preparation with less switching losses and optimized output voltage quality performance. For this purpose the function of inverter is effective manner it is provided by the sinusoidal pulse width modulation technique (SPWM) then the inverter performed accurately and hence the generated required sufficient output voltage with minimized harmonic contents in the output. The conventional out experiments verification that an asymmetrical arrangement delivers closely sinusoidal voltages with very less distortion, using less switching devices. Additionally, torque ripples are significantly reduced.

Index Terms: Multilevel Inverters (Cascade H-Bridge Inverter), DTC (Direct Torque Control), Induction Motor, SPWM.

I. INTRODUCTION

Multilevel voltage-source inverters are deliberate and they are attractively used for high-power and high-voltage applications and customary drives for medium-voltage industrialized applications have become accessible. Solutions by a supplementary number of output voltage levels have the competence to synthesize wave forms through an improved harmonic spectrum and to boundary the motor winding insulation pressure.

Conversely, their cumulative number of devices inclines to diminish the power converter overall performance and reliability. On the other hand, solutions with a less number of levels either essential a moderately large and luxurious *LC* output filters to perimeter the motor winding insulation pressure, or can only be work with motors that do withstand such stress. The several voltage stages have been selected after considering the real-power involvement of the maximum voltage stage. The maximum power delivered by maximum voltage stage is maintained below the required load power. Many techniques have been directed toward improving the

multilevel inverters. Some systems are dealt with advanced topologies, like as cascaded multilevel inverter, to enhance the components utilization and then the asymmetrical multilevel inverter to recover the required output voltage resolution. Other studies focused on developing progressive control approaches or upgrading the voltage source inverter approaches for developing in multilevel inverter. Now symmetrical multilevel inverter, all H-bridge cells are connected by identical voltages, and hence all the arm cells generates related output voltage steps. Conversely, if all the cells are not connected by identical voltages, the inverter becomes an asymmetrical one. In this inverter, the arm cells have dissimilar effect on the generated output voltages. Other techniques are conceivable, like as the neutral point clamped connected by inadequate capacitors. Asymmetrical multilevel inverter has been freshly implemented. In all these considerations, H-bridge technology has been noticed and a variety of assortment of cascaded cell numbers and dc-sources and their ratios has been implemented. The proposed pulse width-modulation (pwm) strategy that maintains the maximum high-voltage stage to function at low frequency conditions the source-voltage assortment.

II. EXISTING SYSTEM

One of the procedures that have been situated by a main multilevel inverter design with direct torque control (DTC),which is predictable today as a high-performance control approach for ac drives. Several authors have noticed the problem of enhancing the performance of DTC ac motors, particularly by decreasing the torque ripple. Various methodologies have been recommended. While these methodologies are well appropriate for the traditional two-levels inverter, their enhancement to greater number of levels is not simple. Throughout this paper, an academic education is used to design a scheme friendly with hybrid cascaded H-bridge multilevel inverter; symmetrical and asymmetrical alignment is employed and verified. Experimental results attained for an asymmetrical inverter-connected induction motor approve the high dynamic presentation of the used technique, presenting good quality and very low torque ripples.

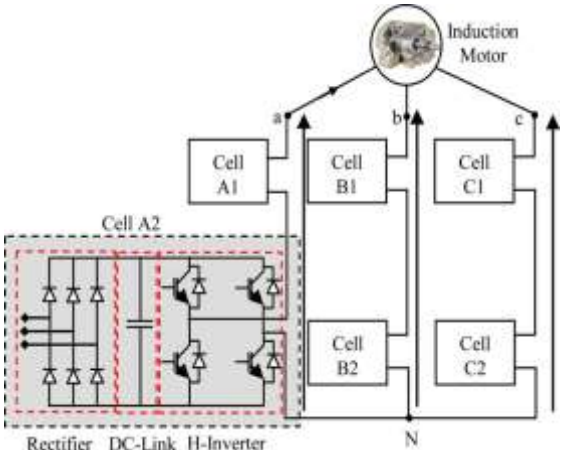

Fig.1. Structure of Two-Cells Cascaded Multilevel Inverter

III. CASCADED H-BRIDGES STRUCTURE AND OPERATION

The cascaded H-bridge inverter contains of power conversion types , each transfers power by difficult to get to dc source on the dc side, which can be learned from fuel cells, batteries, and ultra-capacitors series-connected on the ac side. The benefit of this technology is that the control, modulation and protection necessities of each bridge are segmental. It should be noticed out that, unlike the methods of diode-clamped and flying-capacitor technologies, inaccessible dc sources are mandatory for each cell in each phase. Fig.1demonstrations a three-

phase technology of a cascade inverter with in accessible dc-voltage sources. The produced output phase-voltage waveforms calculated by providing the bridges voltages

$$V_o\ (t) = V_{o,1}(t) + V_{o,2}(t) + \cdots + V_{o,N}(t)\ (1)$$

Where *N* -denotes the number of cascaded bridges. The inverter produced output voltage *VO*(*t*) might be calculated from the separate cells switching conditions

$$V_o\ (t) = \sum_{j=1}^{N}(\mu_j - 1)\, V_{dc,j}, \qquad \mu_j = 0,1,\ldots N\ (2)$$

If all dc-voltage sources in Fig. 1 are identical to *V*dc, the inverters then called it as a symmetric multilevel one. The operative number of produced output voltage levels *n* in symmetric multilevel inverters associated to the cells number by

$$n = 1 + 2N\ \ (3)$$

For example, Fig. 2 illustrated typical waveforms of Fig. 1multilevel inverter with two dc sources (five-levels output). The maximum output response *V*O, Max is then

$$V_{o,MAX} = NV_{dc}\ \ (4)$$

To distribute a huge number of output levels without accumulative the number of inverter parameters, asymmetric multilevel inverters can be applicable.

It is implemented to select the dc-voltage sources considering to a geometric progression with a power factor of 2 or 3.

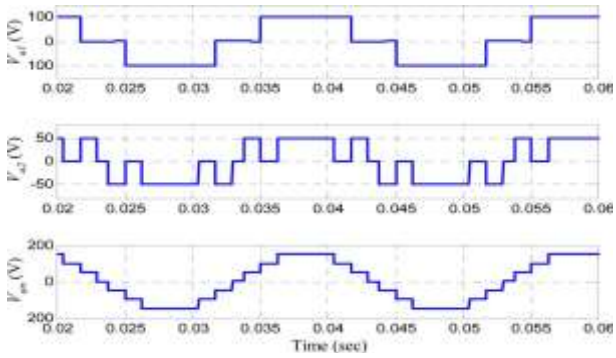

Fig 3 Asymmetric Multilevel Inverter with Seven-Level Output Voltage Synthesis

By using below given method for different voltage levels

$$\begin{cases} n = 2^{N+1} - 1, & if\ V_{dc,j} = 2^{j-1}V_{dc},\ j = 1,2,\ldots N \\ n = 3^N, & if\ V_{dc,j} = 3^{j-1}. \end{cases} \quad \ldots(5)$$

Figs. 3 and 4 demonstrated typical waveforms of Fig.1 multilevel inverter with, individually, two dc sources like *V*acant 2*V*dc for seven-level generated output and two dc sources like *V*dc and3*V*dc for nine-level generated output.

	Symmetrical inverter	Asymmetrical inverter	
		Binary	Ternary
N	$2N+1$	$2^{N+1}-1$	3^N
DC sources number	N	N	N
Switches number	$4N$	$4N$	$4N$
$V_{o,max}$ [pu]	N	2^N-1	$(3^N-1)/2$

Table IComparison of Multilevel Inverters

$V_{o.MAX}=\sum_{j=1}^{N} V_{dc,j}$ ….(6)

Equation (6) can be modified as $\begin{cases} V_{o.MAX} = 2^{N-1}V_{dc,} \; if \; V_{dc,j} = 2^{j-1}V_{dc,} \quad j = 1,2,\dots N \\ V_{o.MAX} = \frac{(3^N-1)}{2} \; V_{dc,} \; if \; V_{dc,j} = 3^{j-1}V_{dc,} \quad j = 1,2,\dots N \end{cases}$ …(7)

Comparing the equations (3) to (7), it can be realized that asymmetrical multilevel inverters can produce more voltage levels and higher maximum generated output voltage with the identical number of bridges. Table I condenses the number of switches, dc sources, levels, and maximum obtainable output voltages for traditional cascaded multilevel inverters methodologies.

Cumulative the number of levels delivers more stages; therefore, the obtainable output voltage will be of sophisticated resolution and the required sinusoidal output voltage can be better achieved. From the *n*3switching operating conditions of *n*-level inverter has zero states, where zero output voltages are created. Next the (*n*3−*n*) nonzero remaining conditions, there are distinctive (unique) states and mutual states.

The unique states deliver voltage vectors that cannot be achieved by any other states. The mutual conditions on the other hand, offered aset of output voltages that can be providing by some other mutual states. The corresponding mutual conditions share the equivalent voltage vectors. The *n*-level inverter can generate [(*n* − 1)3 − (*n* − 1)]nonzero mutual conditions. Fig. 5 exposed the five-level inverter, we can understand the generation of voltage vectors. The number of different voltage vectors acquired from *n*-level inverter is identified by using [*n*3 − (*n* − 1)3].

IV. PROPOSED SYSTEM

The presence of equivalent mutual states has been frequently used to diminish the switching losses. Though, the comparable mutual states can be substituted by any one of these conditions and the other situations can be measured redundant. There are (*n* − 1)3redundant conditions in the *n*-level regular H-bridge multilevel inverter different method to flux-type control. But, in the typical version, significant torque ripple is attained even at high switching frequencies. Furthermore, the inverter sampling frequency is integrally variable and very dependent on shaft speed and torque.

This creates torque distortions within constant frequencies and an acoustic noise with disturbance concentrations very reliant on these mechanical parameters and predominantly harsh at low speed. The supplementary degrees of liberty(space vectors, phase configurations, etc.) delivered by the multilevel inverter must, consequently, be demoralized by the control approach in order to reduce these problems.

V. PROPOSED SPWM TECHNIQUE

SPWM for Multilevel Inverter is founded on classic two level SPWM with triangular carrier and sinusoidal orientation waveform Only difference between two level SPWM and multilevel SPWM is numbers of carriers are used in multilevel SPWM. For ‘m’ level inverter ‘m-1’ carrier are used. Collaboration of particular carrier and reference is utilized to produce gating signal for particular balancing pair of switches in diode clamped or capacitor-clamped inverter or particular cell in multi-cell inverter Carriers utilized in multilevel inverter may be vertically removed or horizontally shifted. Benefit of horizontally shifted carriers scheme is that each modules are switched on and off with a constant number of times by period autonomously of magnitude of produced voltage. But vertically shifted carrier structure can be more easily employed on any digital controller.

Digital operation SPWM method is based on classical SPWM technique with carriers and reference sine waveform. Only change between them is in digital SPWM a sine table comprising of values of sine waveform sampled at certain frequency is utilized. As result reference wave form in digital SPWM characterizes a sample and hold waveform of sine wave forms.

In balanced sampling reference sine waveform is sampled at only positive peak of the carrier waveform and sample is held constant for the whole carrier period. This presents the distortion in modulating signal and phase shift between modulating signal and fundamental component of output voltage. Here sampling frequency is identical to carrier frequency.

5.1 Nomenclature

Vs–denotes the stator voltage vector.

Φs(*φr)*–denotes the stator (rotor) flux vector.

Te-denotes theproducedelectromagnetic torque.

Rs-denotes the internal stator resistance.

Ls-(*Lr) specifies the* stator (rotor) inductance.

*Lm – indicates the m*agnetizing inductance.

*σ – Denotes the t*otal coefficient for leakage, $\sigma = 1 - L2M/LsLr$.

Θsr– indicates Angle between stator and rotor flux vectors.

*P-significant*Pole pair number.

5.2 Torque and Flux Estimation

The flux from the stator vector and an induction motor is integrated to thestator voltage and current vectors by

$$\frac{d\varphi_s}{dt} = V_s\ (t) - R_s\ I_s\ (t) \text{..(8)}$$

Preserving *c*onstant over a switching time interval and ignoring the stator internal resistance, the integration of (10) leads to

$$\Delta\varphi_s\ (t) = \varphi_s\ (t) - \varphi_s\ (t - \Delta t) = \int_{t-\Delta t}^{t} V_s\ \Delta t \ldots \text{(9)}$$

Equation (9) exposes that the stator flux vector is straight affectedby distinctions on the stator voltage vector.

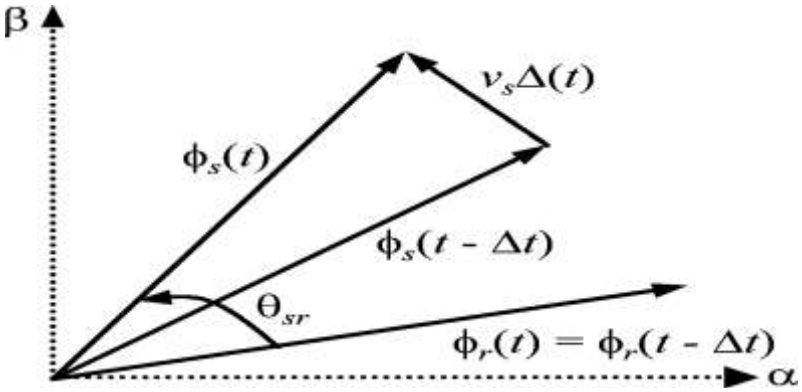

Fig.6 Influence of *Vs.* Over *during* a Simple Interval Δ*t*

On the conflicting, the encouragement of *vs.*over the rotor flux is cleaned by the leakage inductance of rotor and stator, therefore, not suitable over a short-time viewpoint. Meanwhile the stator flux can be altered quickly whereas the rotor flux revolves gentler, the angle between both vectors stator and rotor *θ*sr can be meticulous directly by *vs.* a graphical demonstration of the stator and rotor flux dynamic behavior is exemplified.

The exact correspondence between stator and rotor flux indications that protection the amplitude of *co*nstant will create a constant rotor flux *me*anwhile the electromagnetic torque produced by an induction motor can be calculated by

$$T_e = \frac{3}{2}\frac{L_m}{\sigma L_s L_r}\varphi_s \varphi_r \sin\theta_{sr} \ldots\ldots(10)$$

In *s*owed to the action of *vs.* Permits for direct and quick change in the developed torque. DTC utilizes this standard to complete the induction motor required torque response, by using the suitable stator voltage vector to perfect the flux curve.

5.3 Voltage Vector Selection

Fig. 7 demonstrates one of the 127 voltage vectors created byte inverter at instant=*k*, denoted by *vks.*The next voltage vector, to be active to the load *vk*+1*s*, can be denoted by

$$V_s^{K+1} = V_s^K + \Delta V_s^K \ldots (11)$$

Where Δ*vksrepresents*= *{VI* |*i*= 1,6*}*. Each vector *VI*look liketo one corner of the essential hexagon exemplified in gray andby the dashed line in Fig. 7.

The task is to find which *vk*+1*s* will exact the torqueand flux responses, significant the definite voltage vector *vks*, the measured torque and flux errors as *ekφ*and *ekT*, and the flux of stator vector position is (sector find by angle *θs*).

Note that the next voltage vector *vk*+1*s* functional to the load will continuously be one of the six neighboring vectors to the preceding*vks*; this will soft"n" theswitching effort and decrease high dynamics in torque reaction owing to possible large variations in the position. Table II summa-rises vector assortments for the dissimilar sectors and comparators output (preferred*φs*and *Te*corrections).

To develop the DTC of the induction motor connected by a hybrid cascaded H-bridge multilevel inverter, one must accomplish at each switching period, the inverter switch logic operating conditions as a purpose of the torque and flux immediate values for the assortment of the space vector in the *α–β* surround. The recommended control algorithm was separated into two main responsibilities, which are self-governing and performed in cascade.

VI. CONCLUSION

This paper distributed with a comparison approachment for a cascaded H-bridge multilevel with DTC for induction motor drive. Definitely, balanced and unbalanced provisions of five- and seven-levels-bridge inverters have been associated in order to determine an optimum preparation with less switching losses and augmented output voltage performance.

The accepted out experiments demonstrations that an asymmetrical alignment offers closely sinusoidal voltages with very less distortion, using less switching parameters. For this purpose the function of inverter is effective manner it is provided by the sinusoidal pulse width modulation technique (SPWM) then the inverter performed accurately and hence the generated required sufficient output voltage with minimized harmonic contents in the output. In accretion, torque ripples are significantly minimized: asymmetrical multilevel inverter permits a DTC explanation for high-power induction motor drives, not only owing to the higher voltage competence delivered by multilevel inverters, but fundamentally due to the concentrated switching losses and the enhanced output voltage quality and enactment, which affords sinusoidal current without using of output filter.

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